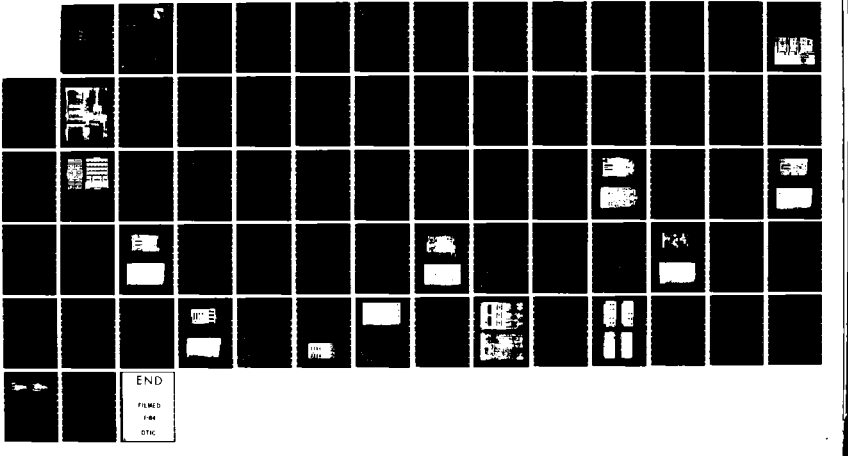
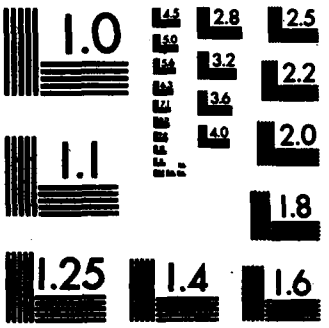
AD-A136 191 THE C-SQUARED SYSTEM: A GENERAL-PURPOSE NEURON NETWORK 1/1
MODEL(U) AIR FORCE AEROSPACE MEDICAL RESEARCH LAB
WRIGHT-PATTERSON AFB OH T C HARTUM ET AL. SEP 83
UNCLASSIFIED AFAMRL-TR-80-84 F/G 17/2 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

AD-A136 191

AFAMRL-TR-80-84

THE C-SQUARED SYSTEM: A GENERAL-PURPOSE NEURON NETWORK MODEL

THOMAS C. HARTRUM
VINCENT D. MORTIMER, JR.
J. RYLAND MUNDIE
DONALD OSBORNE
JAMES C. ROCK

SEPTEMBER 1983

Approved for public release; distribution unlimited

DTIC ELECTE DEC 21 1983 S D E

DTIC FILE COPY

AIR FORCE AEROSPACE MEDICAL RESEARCH LABORATORY
AEROSPACE MEDICAL DIVISION
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

NOTICES

When US Government drawings, specifications, or other data are used for any purpose other than a definitely related Government procurement operation, the Government thereby incurs no responsibility nor any obligation whatsoever, and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise, as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Please do not request copies of this report from Air Force Aerospace Medical Research Laboratory. Additional copies may be purchased from:

National Technical Information Service
5285 Port Royal Road
Springfield, Virginia 22161

Federal Government agencies and their contractors registered with Defense Technical Information Center should direct requests for copies of this report to:

Defense Technical Information Center
Cameron Station
Alexandria, Virginia 22314

TECHNICAL REVIEW AND APPROVAL

AFAMRL-TR-80-84

This report has been reviewed by the Office of Public Affairs (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Henning E. von Gierke

HENNING E. VON GIERKE, Dr Ing
Director
Biodynamics and Bioengineering Division
Air Force Aerospace Medical Research Laboratory

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFAMRL-TR-80-84	2. GOVT ACCESSION NO. AD-A136191	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* The C-Squared System: A General-Purpose Neuron Network Model		5. TYPE OF REPORT & PERIOD COVERED Technical Report 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Thomas C. Hartrum, Vincent D. Mortimer, Jr., J. Ryland Mundie, Donald Osborne and James C. Rock		8. CONTRACT OR GRANT NUMBER(s) N/A
9. PERFORMING ORGANIZATION NAME AND ADDRESS AFAMRL, Biodynamics and Bioengineering Division, AMD, AFSC, Wright-Patterson AFB OH 45433		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62202F, 7231-09-10
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE September, 1983 13. NUMBER OF PAGES 66
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Noise
Noise Environments
Bioenvironmental Noise
Neuron
Neuron Model
Neural Network
Neural Computer

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes a general-purpose neuron network model referred to as the C-squared (C^2) system. The system contains 504 hardware neuron models called syncoders. As the result of an extensive effort to improve these neuron models, five versions (Mod 1 through Mod 5) exist. Regardless of the version, each syncoder circuit board contains two syncoder circuits; and the circuit cards are totally compatible at the board connector interface. The current C^2 System contains some syncoders of all versions. The inputs to each syncoder are fixed bias voltages and weighted pulses from other syncoders. (cont'd)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

Block 20 (cont'd)

These biases and weights are provided by 1,728 sample-and-hold circuits which are set under control of a PDP-8S digital computer. Clearly this provides tremendous flexibility in building complex neuron networks. The ease of constructing such networks is enhanced by providing access to all of the syncoders and sample-and-holds, plus 18 general-purpose operational amplifiers, via three large, removable patch panels. This also allows one to easily change from one complex circuit to another. Discrete components (such as resistors and capacitors) can be connected to the syncoders with special patch cords, modifying the firing characteristics of the individual neuron models. In addition, controls on each syncoder circuit board allow individual neuron thresholds and time constants to be tuned. Since the circuit cards are in slide-out drawers, this can be done while the C^2 System is operating. The C^2 System, itself, is a real-time signal processor; but provisions for patching into any portion of the network allow syncoder outputs to be sampled by a large digital computer for off-line reduction and analysis. Together all of these factors make the C^2 System an extremely flexible tool for studying complex neuron networks.

Currently this system is being used with a special preprocessor called an analog cochlea and with a PDP-11/20 computer to further process and analyze the outputs of the syncoders. Of its many possible applications as a general-purpose signal processor, it has been used to investigate speech recognition and target identification from sonar and doppler radar returns.

SUMMARY

This report describes a general-purpose neuron network model referred to as the C-squared (C^2) system. The system contains 504 hardware neuron models called syncoders. As the result of an extensive effort to improve these neuron models, five versions (Mod 1 through Mod 5) exist. Regardless of the version, each syncoder circuit board contains two syncoder circuits; and the circuit cards are totally compatible at the board connector interface. The current C^2 System contains some syncoders of all versions. The inputs to each syncoder are fixed bias voltages and weighted pulses from other syncoders. These biases and weights are provided by 1,728 sample-and-hold circuits which are set under control of a PDP-8S digital computer. Clearly this provides tremendous flexibility in building complex neuron networks. The ease of constructing such networks is enhanced by providing access to all of the syncoders and sample-and-holds, plus 18 general-purpose operational amplifiers, via three large, removable patch panels. This also allows one to easily change from one complex circuit to another. Discrete components (such as resistors and capacitors) can be connected to the syncoders with special patch cords, modifying the firing characteristics of the individual neuron models. In addition, controls on each syncoder circuit board allow individual neuron thresholds and time constants to be tuned. Since the circuit cards are in slide-out drawers, this can be done while the C^2 System is operating. The C^2 System, itself, is a real-time signal processor; but provisions for patching into any portion of the network allow syncoder outputs to be sampled by a large digital computer for off-line reduction and analysis. Together all of these factors make the C^2 System an extremely flexible tool for studying complex neuron networks.

Currently this sytem is being used with a special preprocessor called an analog cochlea and with a PDP-11/20 computer to further process and analyze the outputs of the syncoders. Of its many possible applications as a general-purpose signal processor, it has been used to investigate speech recognition and target identification from sonar and doppler radar returns.

Accession For	
NTIS GRA&I	X
DTIC TAB	☐
Unannounced	☐
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A-1	

DTIC COPY INSPECTED 3

PREFACE

This report describes the C^3 System hardware as developed over many years. This program was conducted under Project No. 7233, "Applications of Biological Principles as Solutions to Air Force Needs in Signal Processing and Information Handling" and administered initially by the Neurophysiology Branch, then later by the Mathematics and Analysis Branch, Biodynamics and Bioengineering Division of the Air Force Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

The hardware for the C^3 System was developed and fabricated by Systems Research Laboratories, Inc., Dayton, Ohio. This work was accomplished under contracts AF33 (615)-5106, F33615-67-C-1887, F33615-69-C-1683, F33615-70-C-1557, F33615-72-C-1483, and F33615-76-C-0029.

The authors express their thanks to the Air Force Institute of Technology for its support in the integration and preparation of this report.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

INTRODUCTION

Few would argue with the statement that the tremendous information processing capability of mammalian nervous systems results from the parallel processing of information by highly complex elements called neurons. One mainline of neurophysiological research today is the study of mechanisms of information processing exhibited by single neurons and by neural networks of various sizes. The study of neuron networks is an important research area with many potential Air Force applications. These include speech recognition, speaker verification, pattern classification, target recognition, and artificial intelligence. One approach to the study of such networks is to simulate the network on a digital computer. In this arena, one quickly discovers an inverse relationship between the complexity on one's neuron model and the size of simulated neural networks that can be analyzed in a tractable manner. The problem is that even a relatively simple model of the neural transformation, which produces a pulse train from an analog input signal, requires more computer time than the actual events would require. Since the events in a network of neurons may occur simultaneously or be fed back on each other, a network with as few as ten neuron models may easily require two of three orders of magnitude more computing time than the actual physical network would require to perform the same task. A solution to this problem is the use of special hardware neuron models.

Thus, to simulate reasonable-sized neural networks, it is necessary to use a simulation that permits real-time parallel processing. To accomplish this, an experimental computer, the C^3 System, was developed using functional neural models, called syncoders, as the basic computing elements. Each syncoder accepts up to eight inputs, which may be analog signals or pulse trains; and the output of each syncoder is available as both an analog signal and a pulse train. The term "C^3" is not used in the traditional military (i.e. command and control) sense; but instead refers to a computer that is neither purely analog ("A") nor purely digital ("D") but somewhere in between hence, a "C"-type computer and one that, in this latest version, has roughly an order of magnitude increase in the number of functional units over its predecessors.

The principal purpose of this report is to provide detailed hardware descriptions of the components of the C^3 system. Therefore, little detail is included about the historical development of the syncoder concept or of the known information processing capabilities of individual syncoders and networks of syncoders. A complete bibliography of publications relevent to syncoder development and operation is included.

THE SYNCODER CONCEPT

A brief review of syncoder information processing capability is presented here for the convenience of the uninitiated reader. Figure 1 contains a functional block diagram of a syncoder clearly displaying its various components: synapse button, synapse integrator, and encoder. The synapse section of the *syn*coder accepts any combination of up to eight analog signals and/or weighted pulse trains and converts them through the synapse integrator into an analog output signal, S(t). The encoder section of the *syncoder* converts an analog signal, S(t), into an output pulse train by continuously comparing S(t) with an exponentially decaying threshold function, T(t), and producing an output pulse whenever S(t) equals or exceeds T(t). During each output pulse T(t) is reset to its initial value, B, and is allowed to decay exponentially towards zero volts between pulses. In summary, the synapse section accepts pulse trains and analog signals and generates one analog output signal, while the encoder converts that analog output signal into a corresponding pulse train.

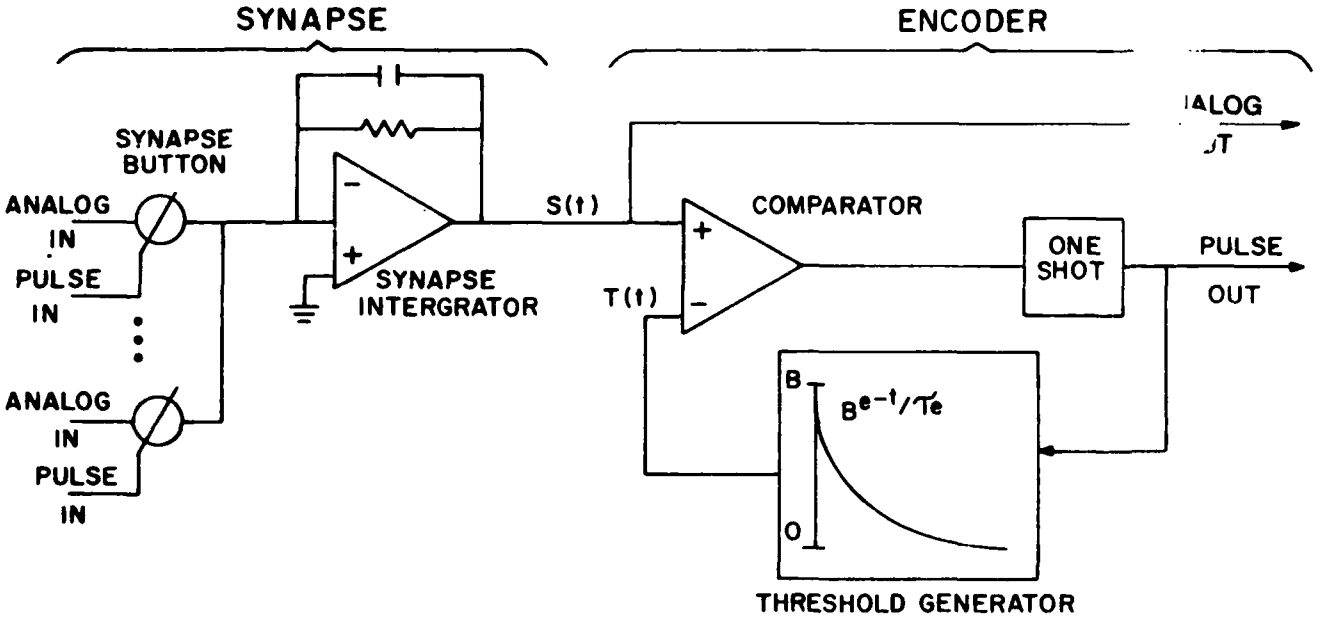


Figure 1. Schematic of a Typical Syncoder Circuit

THE SYNAPSE

The output pulse train of one syncoder may be connected to the synapse input of another syncoder through an analog switch called the synapse button. The synapse button is conceptually equal to a resistor in a series with a switch. During the time that the pulse input to a switch is active, the current resulting from the voltage applied to the analog input is summed with other input currents at the summing junction of the operational amplifier, which charges the feedback capacitor in the synapse integrator. When the pulse input is inactive, the current resulting from the analog input is blocked by the switch so that there is no effect on the synapse integrator. Hence, the analog input to a synapse button may be viewed as a weighting function used to control the effect of a pulse on the following synapse integrator, or the synapse button may be viewed as a gate which permits an analog signal to affect the synapse integrator only during that portion of time when the pulse input is active.

The synapse integrator may be viewed either as a low-pass filter or as a leaky integrator. It sums the currents produced by up to eight analog signals which may or may not be gated by synapse buttons. In practice, it has been found convenient to have at least one DC analog input called a bias signal connected directly through a resistor to each syncoder used in a network. This bias signal can be adjusted so that the encoder does not fire at all in the absence of other input signals, or so that the encoder fires continuously in the absence of other input signals. The reader who is interested in more detailed discussion of synapse function than that given above is referred to Rock (1973) and Mather & Henrichon (1971). In summary, the synapse function serves to provide spatial summation of currents from up to eight different sources, and temporal summation of currents occurring at sequential times.

THE ENCODER

The encoder operates on the analog output signal of the synapse and generates from it an output pulse train. One feature of this nonlinear encoding operation is exhibited by the encoder response to a DC input signal, S(t) = S. In this case, an output pulse is generated each time the exponentially decaying threshold function equals the input signal and periodic pulse train results. Expressing this with the mathematical relationship $S = B[\exp(-I/\tau)]$ and rearranging terms, it can be shown that the interpulse interval, I, is a logarithmic function of the input signal amplitude, S, and the threshold initial value, B, and directly proportional to the threshold decay time constant, τ.

$$I = \tau \ln(B/S) \qquad \text{for } S < B$$

For periodic input signals, S(t) = S(t + T), the encoder generates a periodic output pulse train. Depending upon the parameters of the encoder and the signal, the pulse train may be periodic with the same period as the input or integer multiples of the input period. The phenomenon of periodic output pulse patterns phaselocking to sinusoidal input signals was reported by Ziskin and Mundie (1971). The transient approach to stable phase locking and the conditions for phase locking to arbitrary periodic input signals were reported by Rock (1973). For the purpose of this report, the response of an encoder to a periodic input signal is generally not a sequence of uniformly spaced pulses. It is, rather, a repeating pattern of a finite sequence of pulses.

Because of the nonlinear nature of the syncoder transfer function, there is no general analysis technique for predicting the output pulse sequence given an arbitrary, nonperiodic input waveform. Since in the natural environment of information processing, periodic events are the exception rather than the rule, it is necessary to fabricate syncoders and study their behavior with nonperiodic inputs, using hardware devices, rather than to program a digital computer to simulate mathematical models.

THE C² SYSTEM

The C² System consists of a control system and three large bays with patch panels and the associated circuitry for programming large syncoder networks. Figure 2 is a photograph of the system showing, from left to right, network bays 1, 2, and 3, and the control system bay with its teletypewriter in the foreground.

Figure 2. Primary Hardware Units of the C² System

Each bay contains 168 syncoder circuits, 576 sample-and-hold circuits, and 6 individual operational amplifier circuits. The large red, white, green, and gray patch panels and a variety of plugable components allow programmed interconnection of these circuits to simulate large syncoder networks. The large patch panels are removable so that several different syncoder networks may be programmed at any one time. The system may be reconfigured simply by interchanging the preprogrammed patch panels.

The primary function of the control system is to sequence analog voltages to and from the syncoder network simulation bays. Up to 1728 output voltage channels and up to 512 input voltage channels may be addressed. The control system contains a PDP-8S computer, input/output (I/O) control logic, and analog signal conditioning circuits.

The relays on the sample-and-hold boards are all connected to the analog output bus of the control system's output multiplexer digital-to-analog (D-A) converter. Under program control, the PDP-8S can selectively close these relays one at a time and set a stored voltage in each of the sample-and-hold circuits. In a similar manner, the relays on the syncoder boards are connected to the analog input bus of the input multiplexer analog-to-digital (A-D) converter. Under program control, the PDP-8S can selectively close these relays one at a time and record the analog output voltage of each of the syncoder circuits. The converter can be manually set to operate at any resolution between 6 and 12 bits.

There are two main programs for the PDP-8S which are used with the C^2 System. SYNSET is the program used to control syncoder network operation. The program provides for loading voltages into all sample-and-hold circuits, or any subset of them, and for reading syncoder analog output voltages for all or any subset of the syncoders in C^2. A program called DALE, when used with its patch panel, serves to verify operation of all sample-and-hold boards, syncoder boards, input and output matrix drivers, and A-D and D-A converters. DALE is used to detect and locate malfunctioning circuit boards.

THE CONTROL BAY

Figure 3 is a block digram of the important elements of the control system. Under program control, the PDP-8S can load analog voltages into the sample-and-hold circuits in the bays through the output multiplexer, or read and store the value of the analog output voltage from any syncoder board in the bays through the input multiplexer. The real-time clocks serve to control the dwell time of the reed relays used to select the signal source and destination. The control logic serves to decode binary addresses supplied by the computer and to activate the proper pair of driver circuits to close one and only one relay in the appropriate relay matrix. The ASR 33 teletypewriter permits the operator to feed instructions to the PDP-8S and to receive lists of analog voltages measured on network syncoders through the input multiplexer. Programs to control system operation may be loaded from magnetic tape

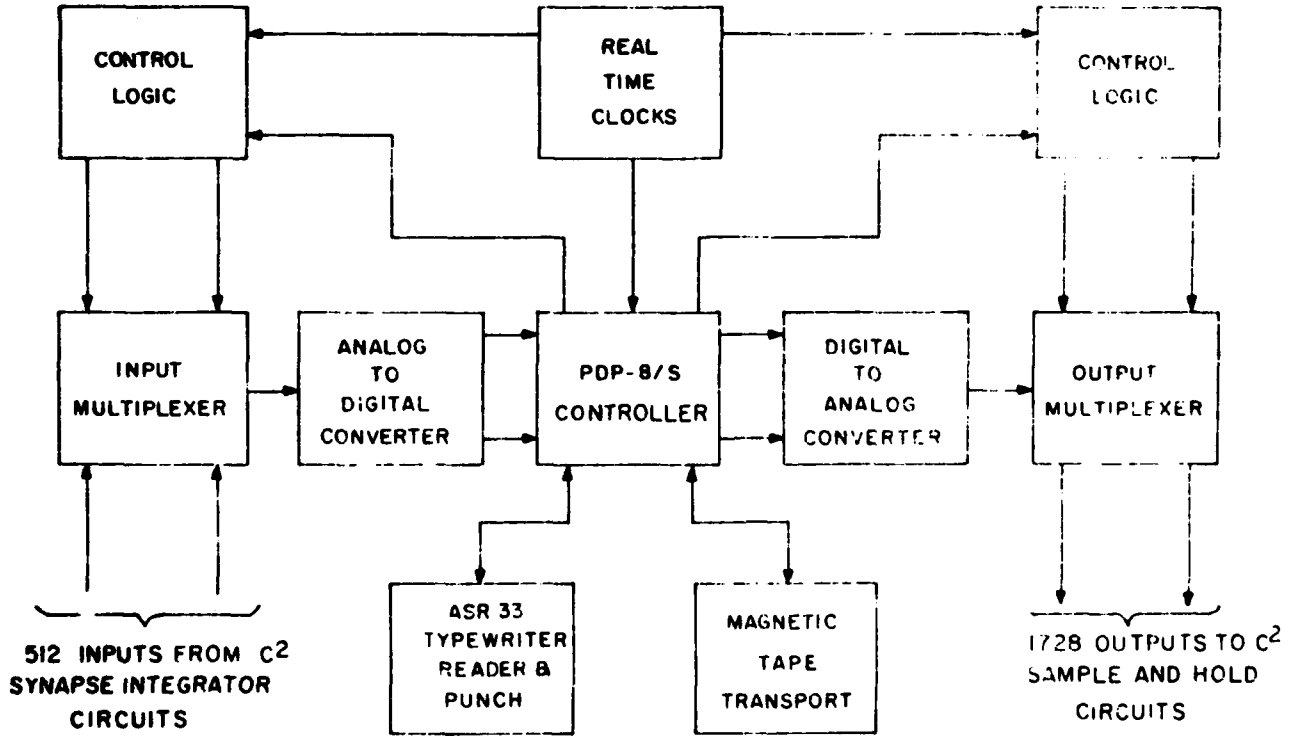


Figure 3. Block Diagram of the C^2 System Control Units

through the tape transport unit, from paper tape or from the keyboard through the teletypewriter, or manually through the PDP-8S console switch register. The only system function not under program control is the output multiplexer real-time clock. Its period is continuously variable from 5 to 50 milliseconds by means of the rotary knob located on the I/O status panel. The input multiplexer real-time clock runs at a fixed period of 4 milliseconds.

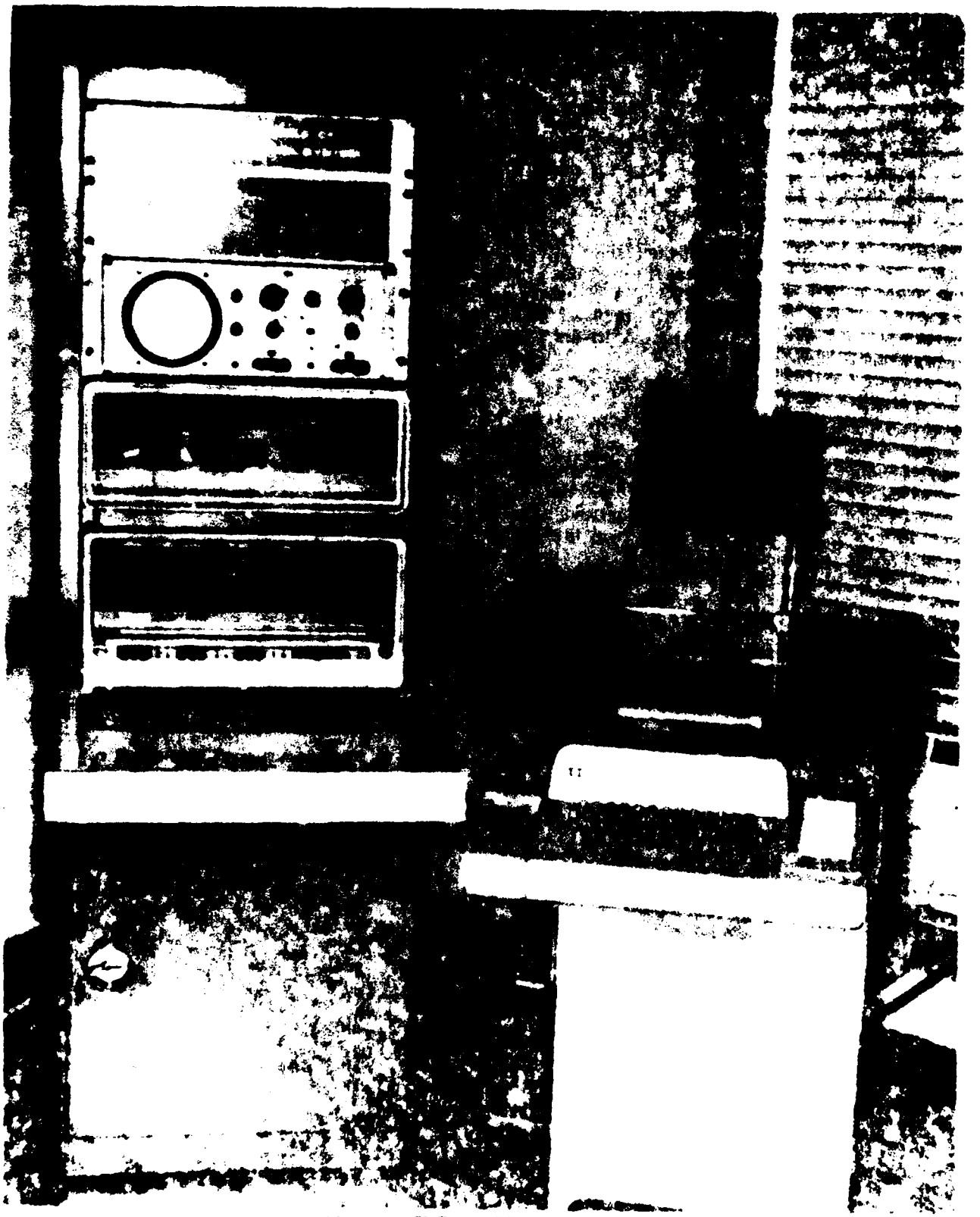


Figure 4. C³ Control Bay and Teletypewriter

The interface system control bay is mobile, and may be positioned up to 20 feet from the C³ network bays. Four cables are required to connect the C³ controller with the bays. The green multi-wire cable connects J2 (jack number 2) of the control cabinet with the C³ output relay matrix. The output relays are located on the sample-and-hold circuit boards. The orange multi-wire cable connects J1 of the control cabinet to the C³ input relay matrix. The input relays are mounted on syncoder circuits boards and connected to synapse integrator outputs. One twinax cable connects J3 with the C³ input relay matrix analog signal bus, the other twinax cable connects J4 with the C³ output relay matrix analog signal bus.

Figure 4 shows the C³ control system cabinet. It shows, from top to bottom, the I/O control logic status indicator panel, a system monitoring oscilloscope, the A-D converter, and the PDP-8S computer.

The top row of 12 lights on the I/O indicator panel is the output address indicator. It contains a 12-bit binary version of the output address register. This address determines which of the 1728 sample-and-hold relays in the network bays is closed. The relays are physically located on the sample-and-hold boards discussed later in this report. The bays are wired in such a manner that each of the 1728 output relays is located at a junction point within a 27 by 64 area of a 32 by 64 matrix. Figure 5 shows a block diagram of the logic used to convert this binary address into a single relay closure. Each relay junction point is addressable by activation of the appropriate negative and positive relay driver lines. The bit positions are labeled 0 through 11 from left to right with bit 0 being the most significant bit. In the decoding operation bit 0 is ignored, bits 1 through 5 are decoded into a signal required to activate one of the 32 positive line drivers, and bits 6 through 11 are decoded into the signal required to activate one of the 64 negative line drivers. The 32 positive and 64 negative line drivers are used to activate a diode matrix with the relay coils in series with the diodes in such a manner that one relay is closed in the matrix for each address generated by the computer. Table 1 contains the overall relationship between the output address (read in octal) and the physical location of the associated sample-and-hold circuit in the C³ network bays.

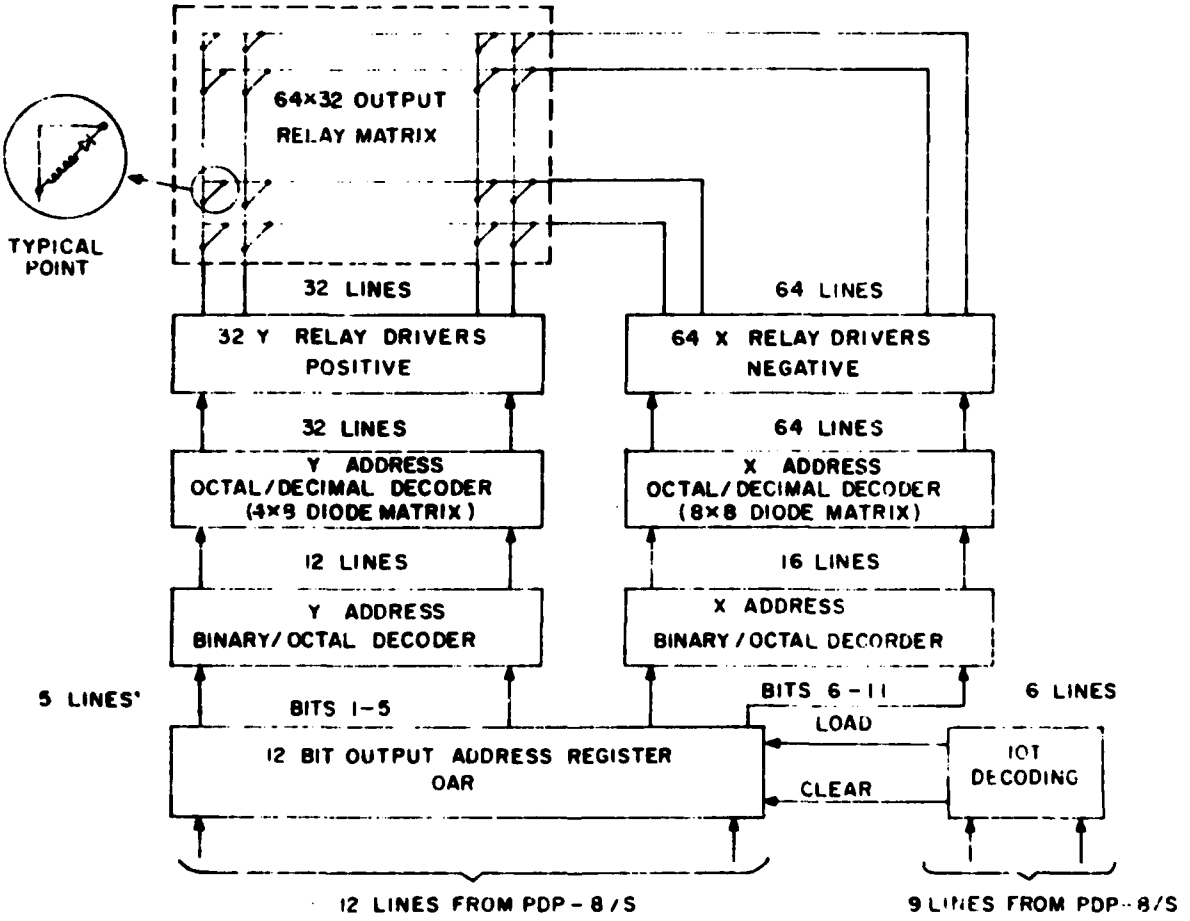


Figure 5. Block Diagram of the Controller Output Multiplexer

Table 1. Sample-and-Hold Locations Related to Controller Output Addresses

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 00	01	02	03	04	05	06	07
00	1A1A	1A1B	1A1C	1A1D	1A1E	1A1F	1A1G	1A1H
01	1A3S	1A3T	1A3U	1A3V	1A3W	1A3X	1A3Y	1A3Z
02	1B2J	1B2K	1B2L	1B2M	1B2N	1B2P	1B2Q	1B2R
03	1C1A	1C1B	1C1C	1C1D	1C1E	1C1F	1C1G	1C1H
04	1C3S	1C3T	1C3U	1C3V	1C3W	1C3X	1C3Y	1C3Z
05	1D2J	1D2K	1D2L	1D2M	1D2N	1D2P	1D2Q	1D2R
06	1E1A	1E1B	1E1C	1E1D	1E1E	1E1F	1E1G	1E1H
07	1E3S	1E3T	1E3U	1E3V	1E3W	1E3X	1E3Y	1E3Z
10	1F2J	1F2K	1F2L	1F2M	1F2N	1F2P	1F2Q	1F2R
11	2A1A	2A1B	2A1C	2A1D	2A1E	2A1F	2A1G	2A1H
12	2A3S	2A3T	2A3U	2A3V	2A3W	2A3X	2A3Y	2A3Z
13	2B2J	2B2K	2B2L	2B2M	2B2N	2B2P	2B2Q	2B2R
14	2C1A	2C1B	2C1C	2C1D	2C1E	2C1F	2C1G	2C1H
15	2C3S	2C3T	2C3U	2C3V	2C3W	2C3X	2C3Y	2C3Z
16	2D2J	2D2K	2D2L	2D2M	2D2N	2D2P	2D2Q	2D2R
17	2E1A	2E1B	2E1C	2E1D	2E1E	2E1F	2E1G	2E1H
20	2E3S	2E3T	2E3U	2E3V	2E3W	2E3X	2E3Y	2E3Z
21	2F2J	2F2K	2F2L	2F2M	2F2N	2F2P	2F2Q	2F2R
22	3A1A	3A1B	3A1C	3A1D	3A1E	3A1F	3A1G	3A1H
23	3A3S	3A3T	3A3U	3A3V	3A3W	3A3X	3A3Y	3A3Z
24	3B2J	3B2K	3B2L	3B2M	3B2N	3B2P	3B2Q	3B2R
25	3C1A	3C1B	3C1C	3C1D	3C1E	3C1F	3C1G	3C1H
26	3C3S	3C3T	3C3U	3C3V	3C3W	3C3X	3C3Y	3C3Z
27	3D2J	3D2K	3D2L	3D2M	3D2N	3D2P	3D2Q	3D2R
30	3E1A	3E1B	3E1C	3E1D	3E1E	3E1F	3E1G	3E1H
31	3E3S	3E3T	3E3U	3E3V	3E3W	3E3X	3E3Y	3E3Z
32	3F2J	3F2K	3F2L	3F2M	3F2N	3F2P	3F2Q	3F2R

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 10	11	12	13	14	15	16	17
00	1A1J	1A1K	1A1L	1A1M	1A1N	1A1P	1A1Q	1A1R
01	1A4A	1A4B	1A4C	1A4D	1A4E	1A4F	1A4G	1A4H
02	1B2S	1B2T	1B2U	1B2V	1B2W	1B2X	1B2Y	1B2Z
03	1C1J	1C1K	1C1L	1C1M	1C1N	1C1P	1C1Q	1C1R
04	1C4A	1C4B	1C4C	1C4D	1C4E	1C4F	1C4G	1C4H
05	1D2S	1D2T	1D2U	1D2V	1D2W	1D2X	1D2Y	1D2Z
06	1E1J	1E1K	1E1L	1E1M	1E1N	1E1P	1E1Q	1E1R
07	1E4A	1E4B	1E4C	1E4D	1E4E	1E4F	1E4G	1E4H
10	1F2S	1F2T	1F2U	1F2V	1F2W	1F2X	1F2Y	1F2Z
11	2A1J	2A1K	2A1L	2A1M	2A1N	2A1P	2A1Q	2A1R
12	2A4A	2A4B	2A4C	2A4D	2A4E	2A4F	2A4G	2A4H
13	2B2S	2B2T	2B2U	2B2V	2B2W	2B2X	2B2Y	2B2Z
14	2C1J	2C1K	2C1L	2C1M	2C1N	2C1P	2C1Q	2C1R
15	2C4A	2C4B	2C4C	2C4D	2C4E	2C4F	2C4G	2C4H
16	2D2S	2D2T	2D2U	2D2V	2D2W	2D2X	2D2Y	2D2Z
17	2E1J	2E1K	2E1L	2E1M	2E1N	2E1P	2E1Q	2E1R
20	2E4A	2E4B	2E4C	2E4D	2E4E	2E4F	2E4G	2E4H
21	2F2S	2F2T	2F2U	2F2V	2F2W	2F2X	2F2Y	2F2Z
22	3A1J	3A1K	3A1L	3A1M	3A1N	3A1P	3A1Q	3A1R
23	3A4A	3A4B	3A4C	3A4D	3A4E	3A4F	3A4G	3A4H
24	3B2S	3B2T	3B2U	3B2V	3B2W	3B2X	3B2Y	3B2Z
25	3C1J	3C1K	3C1L	3C1M	3C1N	3C1P	3C1Q	3C1R
26	3C4A	3C4B	3C4C	3C4D	3C4E	3C4F	3C4G	3C4H
27	3D2S	3D2T	3D2U	3D2V	3D2W	3D2X	3D2Y	3D2Z
30	3E1J	3E1K	3E1L	3E1M	3E1N	3E1P	3E1Q	3E1R
31	3E4A	3E4B	3E4C	3E4D	3E4E	3E4F	3E4G	3E4H
32	3F2S	3F2T	3F2U	3F2V	3F2W	3F2X	3F2Y	3F2Z

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 20	21	22	23	24	25	26	27
00	1A1S	1A1T	1A1U	1A1V	1A1W	1A1X	1A1Y	1A1Z
01	1A4J	1A4K	1A4L	1A4M	1A4N	1A4P	1A4Q	1A4R
02	1B3A	1B3B	1B3C	1B3D	1B3E	1B3F	1B3G	1B3H
03	1C1S	1C1T	1C1U	1C1V	1C1W	1C1X	1C1Y	1C1Z
04	1C4J	1C4K	1C4L	1C4M	1C4N	1C4P	1C4Q	1C4R
05	1D3A	1D3B	1D3C	1D3D	1D3E	1D3F	1D3G	1D3H
06	1E1S	1E1T	1E1U	1E1V	1E1W	1E1X	1E1Y	1E1Z
07	1E4J	1E4K	1E4L	1E4M	1E4N	1E4P	1E4Q	1E4R
10	1F3A	1F3B	1F3C	1F3D	1F3E	1F3F	1F3G	1F3H
11	2A1S	2A1T	2A1U	2A1V	2A1W	2A1X	2A1Y	2A1Z
12	2A4J	2A4K	2A4L	2A4M	2A4N	2A4P	2A4Q	2A4R
13	2B3A	2B3B	2B3C	2B3D	2B3E	2B3F	2B3G	2B3H
14	2C1S	2C1T	2C1U	2C1V	2C1W	2C1X	2C1Y	2C1Z
15	2C4J	2C4K	2C4L	2C4M	2C4N	2C4P	2C4Q	2C4R
16	2D3A	2D3B	2D3C	2D3D	2D3E	2D3F	2D3G	2D3H
17	2E1S	2E1T	2E1U	2E1V	2E1W	2E1X	2E1Y	2E1Z
20	2E4J	2E4K	2E4L	2E4M	2E4N	2E4P	2E4Q	2E4R
21	2F3A	2F3B	2F3C	2F3D	2F3E	2F3F	2F3G	2F3H
22	3A1S	3A1T	3A1U	3A1V	3A1W	3A1X	3A1Y	3A1Z
23	3A4J	3A4K	3A4L	3A4M	3A4N	3A4P	3A4Q	3A4R
24	3B3A	3B3B	3B3C	3B3D	3B3E	3B3F	3B3G	3B3H
25	3C1S	3C1T	3C1U	3C1V	3C1W	3C1X	3C1Y	3C1Z
26	3C4J	3C4K	3C4L	3C4M	3C4N	3C4P	3C4Q	3C4R
27	3D3A	3D3B	3D3C	3D3D	3D3E	3D3F	3D3G	3D3H
30	3E1S	3E1T	3E1U	3E1V	3E1W	3E1X	3E1Y	3E1Z
31	3E4J	3E4K	3E4L	3E4M	3E4N	3E4P	3E4Q	3E4R
32	3F3A	3F3B	3F3C	3F3D	3F3E	3F3F	3F3G	3F3H

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 30	31	32	33	34	35	36	37
00	1A2A	1A2B	1A2C	1A2D	1A2E	1A2F	1A2G	1A2H
01	1A4S	1A4T	1A4U	1A4V	1A4W	1A4X	1A4Y	1A4Z
02	1B3J	1B3K	1B3L	1B3M	1B3N	1B3P	1B3Q	1B3R
03	1C2A	1C2B	1C2C	1C2D	1C2E	1C2F	1C2G	1C2H
04	1C4S	1C4T	1C4U	1C4V	1C4W	1C4X	1C4Y	1C4Z
05	1D3J	1D3K	1D3L	1D3M	1D3N	1D3P	1D3Q	1D3R
06	1E2A	1E2B	1E2C	1E2D	1E2E	1E2F	1E2G	1E2H
07	1E4S	1E4T	1E4U	1E4V	1E4W	1E4X	1E4Y	1E4Z
10	1F3J	1F3K	1F3L	1F3M	1F3N	1F3P	1F3Q	1F3R
11	2A2A	2A2B	2A2C	2A2D	2A2E	2A2F	2A2G	2A2H
12	2A4S	2A4T	2A4U	2A4V	2A4W	2A4X	2A4Y	2A4Z
13	2B3J	2B3K	2B3L	2B3M	2B3N	2B3P	2B3Q	2B3R
14	2C2A	2C2B	2C2C	2C2D	2C2E	2C2F	2C2G	2C2H
15	2C4S	2C4T	2C4U	2C4V	2C4W	2C4X	2C4Y	2C4Z
16	2D3J	2D3K	2D3L	2D3M	2D3N	2D3P	2D3Q	2D3R
17	2E2A	2E2B	2E2C	2E2D	2E2E	2E2F	2E2G	2E2H
20	2E4S	2E4T	2E4U	2E4V	2E4W	2E4X	2E4Y	2E4Z
21	2F3J	2F3K	2F3L	2F3M	2F3N	2F3P	2F3Q	2F3R
22	3A2A	3A2B	3A2C	3A2D	3A2E	3A2F	3A2G	3A2H
23	3A4S	3A4T	3A4U	3A4V	3A4W	3A4X	3A4Y	3A4Z
24	3B3J	3B3K	3B3L	3B3M	3B3N	3B3P	3B3Q	3B3R
25	3C2A	3C2B	3C2C	3C2D	3C2E	3C2F	3C2G	3C2H
26	3C4S	3C4T	3C4U	3C4V	3C4W	3C4X	3C4Y	3C4Z
27	3D3J	3D3K	3D3L	3D3M	3D3N	3D3P	3D3Q	3D3R
30	3E2A	3E2B	3E2C	3E2D	3E2E	3E2F	3E2G	3E2H
31	3E4S	3E4T	3E4U	3E4V	3E4W	3E4X	3E4Y	3E4Z
32	3F3J	3F3K	3F3L	3F3M	3F3N	3F3P	3F3Q	3F3R

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 40	41	42	43	44	45	46	47
00	1A2J	1A2K	1A2L	1A2M	1A2N	1A2P	1A2Q	1A2R
01	1B1A	1B1B	1B1C	1B1D	1B1E	1B1F	1B1G	1B1H
02	1B3S	1B3T	1B3U	1B3V	1B3W	1B3X	1B3Y	1B3Z
03	1C2J	1C2K	1C2L	1C2M	1C2N	1C2P	1C2Q	1C2R
04	1D1A	1D1B	1D1C	1D1D	1D1E	1D1F	1D1G	1D1H
05	1D3S	1D3T	1D3U	1D3V	1D3W	1D3X	1D3Y	1D3Z
06	1E2J	1E2K	1E2L	1E2M	1E2N	1E2P	1E2Q	1E2R
07	1F1A	1F1B	1F1C	1F1D	1F1E	1F1F	1F1G	1F1H
10	1F3S	1F3T	1F3U	1F3V	1F3W	1F3X	1F3Y	1F3Z
11	2A2J	2A2K	2A2L	2A2M	2A2N	2A2P	2A2Q	2A2R
12	2B1A	2B1B	2B1C	2B1D	2B1E	2B1F	2B1G	2B1H
13	2B3S	2B3T	2B3U	2B3V	2B3W	2B3X	2B3Y	2B3Z
14	2C2J	2C2K	2C2L	2C2M	2C2N	2C2P	2C2Q	2C2R
15	2D1A	2D1B	2D1C	2D1D	2D1E	2D1F	2D1G	2D1H
16	2D3S	2D3T	2D3U	2D3V	2D3W	2D3X	2D3Y	2D3Z
17	2E2J	2E2K	2E2L	2E2M	2E2N	2E2P	2E2Q	2E2R
20	2F1A	2F1B	2F1C	2F1D	2F1E	2F1F	2F1G	2F1H
21	2F3S	2F3T	2F3U	2F3V	2F3W	2F3X	2F3Y	2F3Z
22	3A2J	3A2K	3A2L	3A2M	3A2N	3A2P	3A2Q	3A2R
23	3B1A	3B1B	3B1C	3B1D	3B1E	3B1F	3B1G	3B1H
24	3B3S	3B3T	3B3U	3B3V	3B3W	3B3X	3B3Y	3B3Z
25	3C2J	3C2K	3C2L	3C2M	3C2N	3C2P	3C2Q	3C2R
26	3D1A	3D1B	3D1C	3D1D	3D1E	3D1F	3D1G	3D1H
27	3D3S	3D3T	3D3U	3D3V	3D3W	3D3X	3D3Y	3D3Z
30	3E2J	3E2K	3E2L	3E2M	3E2N	3E2P	3E2Q	3E2R
31	3F1A	3F1B	3F1C	3F1D	3F1E	3F1F	3F1G	3F1H
32	3F3S	3F3T	3F3U	3F3V	3F3W	3F3X	3F3Y	3F3Z

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 50	51	52	53	54	55	56	57
00	1A2S	1A2T	1A2U	1A2V	1A2W	1A2X	1A2Y	1A2Z
01	1B1J	1B1K	1B1L	1B1M	1B1N	1B1P	1B1Q	1B1R
02	1B4A	1B4B	1B4C	1B4D	1B4E	1B4F	1B4G	1B4H
03	1C2S	1C2T	1C2U	1C2V	1C2W	1C2X	1C2Y	1C2Z
04	1D1J	1D1K	1D1L	1D1M	1D1N	1D1P	1D1Q	1D1R
05	1D4A	1D4B	1D4C	1D4D	1D4E	1D4F	1D4G	1D4H
06	1E2S	1E2T	1E2U	1E2V	1E2W	1E2X	1E2Y	1E2Z
07	1F1J	1F1K	1F1L	1F1M	1F1N	1F1P	1F1Q	1F1R
10	1F4A	1F4B	1F4C	1F4D	1F4E	1F4F	1F4G	1F4H
11	2A2S	2A2T	2A2U	2A2V	2A2W	2A2X	2A2Y	2A2Z
12	2B1J	2B1K	2B1L	2B1M	2B1N	2B1P	2B1Q	2B1R
13	2B4A	2B4B	2B4C	2B4D	2B4E	2B4F	2B4G	2B4H
14	2C2S	2C2T	2C2U	2C2V	2C2W	2C2X	2C2Y	2C2Z
15	2D1J	2D1K	2D1L	2D1M	2D1N	2D1P	2D1Q	2D1R
16	2D4A	2D4B	2D4C	2D4D	2D4E	2D4F	2D4G	2D4H
17	2E2S	2E2T	2E2U	2E2V	2E2W	2E2X	2E2Y	2E2Z
20	2F1J	2F1K	2F1L	2F1M	2F1N	2F1P	2F1Q	2F1R
21	2F4A	2F4B	2F4C	2F4D	2F4E	2F4F	2F4G	2F4H
22	3A2S	3A2T	3A2U	3A2V	3A2W	3A2X	3A2Y	3A2Z
23	3B1J	3B1K	3B1L	3B1M	3B1N	3B1P	3B1Q	3B1R
24	3B4A	3B4B	3B4C	3B4D	3B4E	3B4F	3B4G	3B4H
25	3C2S	3C2T	3C2U	3C2V	3C2W	3C2X	3C2Y	3C2Z
26	3D1J	3D1K	3D1L	3D1M	3D1N	3D1P	3D1Q	3D1R
27	3D4A	3D4B	3D4C	3D4D	3D4E	3D4F	3D4G	3D4H
30	3E2S	3E2T	3E2U	3E2V	3E2W	3E2X	3E2Y	3E2Z
31	3F1J	3F1K	3F1L	3F1M	3F1N	3F1P	3F1Q	3F1R
32	3F4A	3F4B	3F4C	3F4D	3F4E	3F4F	3F4G	3F4H

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 60	61	62	63	64	65	66	67
00	1A3A	1A3B	1A3C	1A3D	1A3E	1A3F	1A3G	1A3H
01	1B1S	1B1T	1B1U	1B1V	1B1W	1B1X	1B1Y	1B1Z
02	1B4J	1B4K	1B4L	1B4M	1B4N	1B4P	1B4Q	1B4R
03	1C3A	1C3B	1C3C	1C3D	1C3E	1C3F	1C3G	1C3H
04	1D1S	1D1T	1D1U	1D1V	1D1W	1D1X	1D1Y	1D1Z
05	1D4J	1D4K	1D4L	1D4M	1D4N	1D4P	1D4Q	1D4R
06	1E3A	1E3B	1E3C	1E3D	1E3E	1E3F	1E3G	1E3H
07	1F1S	1F1T	1F1U	1F1V	1F1W	1F1X	1F1Y	1F1Z
10	1F4J	1F4K	1F4L	1F4M	1F4N	1F4P	1F4Q	1F4R
11	2A3A	2A3B	2A3C	2A3D	2A3E	2A3F	2A3G	2A3H
12	2B1S	2B1T	2B1U	2B1V	2B1W	2B1X	2B1Y	2B1Z
13	2B4J	2B4K	2B4L	2B4M	2B4N	2B4P	2B4Q	2B4R
14	2C3A	2C3B	2C3C	2C3D	2C3E	2C3F	2C3G	2C3H
15	2D1S	2D1T	2D1U	2D1V	2D1W	2D1X	2D1Y	2D1Z
16	2D4J	2D4K	2D4L	2D4M	2D4N	2D4P	2D4Q	2D4R
17	2E3A	2E3B	2E3C	2E3D	2E3E	2E3F	2E3G	2E3H
20	2F1S	2F1T	2F1U	2F1V	2F1W	2F1X	2F1Y	2F1Z
21	2F4J	2F4K	2F4L	2F4M	2F4N	2F4P	2F4Q	2F4R
22	3A3A	3A3B	3A3C	3A3D	3A3E	3A3F	3A3G	3A3H
23	3B1S	3B1T	3B1U	3B1V	3B1W	3B1X	3B1Y	3B1Z
24	3B4J	3B4K	3B4L	3B4M	3B4N	3B4P	3B4Q	3B4R
25	3C3A	3C3B	3C3C	3C3D	3C3E	3C3F	3C3G	3C3H
26	3D1S	3D1T	3D1U	3D1V	3D1W	3D1X	3D1Y	3D1Z
27	3D4J	3D4K	3D4L	3D4M	3D4N	3D4P	3D4Q	3D4R
30	3E3A	3E3B	3E3C	3E3D	3E3E	3E3F	3E3G	3E3H
31	3F1S	3F1T	3F1U	3F1V	3F1W	3F1X	3F1Y	3F1Z
32	3F4J	3F4K	3F4L	3F4M	3F4N	3F4P	3F4Q	3F4R

Table 1. Sample-and-Hold Locations Related to Controller Output Adresses (Continued)

OUTPUT ADDRESSES Positive (Bits 1-5)	Negative (Bits 6-11) 70	71	72	73	74	75	76	77
00	1A3J	1A3K	1A3L	1A3M	1A3N	1A3P	1A3Q	1A3R
01	1B2A	1B2B	1B2C	1B2D	1B2E	1B2F	1B2G	1B2H
02	1B4S	1B4T	1B4U	1B4V	1B4W	1B4X	1B4Y	1B4Z
03	1C3J	1C3K	1C3L	1C3M	1C3N	1C3P	1C3Q	1C3R
04	1D2A	1D2B	1D2C	1D2D	1D2E	1D2F	1D2G	1D2H
05	1D4S	1D4T	1D4U	1D4V	1D4W	1D4X	1D4Y	1D4Z
06	1E3J	1E3K	1E3L	1E3M	1E3N	1E3P	1E3Q	1E3R
07	1F2A	1F2B	1F2C	1F2D	1F2E	1F2F	1F2G	1F2H
10	1F4S	1F4T	1F4U	1F4V	1F4W	1F4X	1F4Y	1F4Z
11	2A3J	2A3K	2A3L	2A3M	2A3N	2A3P	2A3Q	2A3R
12	2B2A	2B2B	2B2C	2B2D	2B2E	2B2F	2B2G	2B2H
13	2B4S	2B4T	2B4U	2B4V	2B4W	2B4X	2B4Y	2B4Z
14	2C3J	2C3K	2C3L	2C3M	2C3N	2C3P	2C3Q	2C3R
15	2D2A	2D2B	2D2C	2D2D	2D2E	2D2F	2D2G	2D2H
16	2D4S	2D4T	2D4U	2D4V	2D4W	2D4X	2D4Y	2D4Z
17	2E3J	2E3K	2E3L	2E3M	2E3N	2E3P	2E3Q	2E3R
20	2F2A	2F2B	2F2C	2F2D	2F2E	2F2F	2F2G	2F2H
21	2F4S	2F4T	2F4U	2F4V	2F4W	2F4X	2F4Y	2F4Z
22	3A3J	3A3K	3A3L	3A3M	3A3N	3A3P	3A3Q	3A3R
23	3B2A	3B2B	3B2C	3B2D	3B2E	3B2F	3B2G	3B2H
24	3B4S	3B4T	3B4U	3B4V	3B4W	3B4X	3B4Y	3B4Z
25	3C3J	3C3K	3C3L	3C3M	3C3N	3C3P	3C3Q	3C3R
26	3D2A	3D2B	3D2C	3D2D	3D2E	3D2F	3D2G	3D2H
27	3D4S	3D4T	3D4U	3D4V	3D4W	3D4X	3D4Y	3D4Z
30	3E3J	3E3K	3E3L	3E3M	3E3N	3E3P	3E3Q	3E3R
31	3F2A	3F2B	3F2C	3F2D	3F2E	3F2F	3F2G	3F2H
32	3F4S	3F4T	3F4U	3F4V	3F4W	3F4X	3F4Y	3F4Z

The row of eight lights below the output address indicator is the D-A converter indicator. It shows an 8-bit binary number equal to the contents of the D-A converter register. Table 2 contains the conversion between values of this binary number and the analog output voltage which may be any one of 255 levels between + 10 and − 10 volts.

Table 2. Representative Digital-to-Analog Conversions for Sample-and-Hold Voltages

Displayed No. in Octal	Voltage	Displayed No. in Octal	Voltage
000	0.000	200	+ 10.000
001	− 0.079	201	+ 9.921
002	− 0.157	202	+ 9.843
—	—	—	—
—	—	—	—
—	—	—	—
007	− 0.551	207	+ 9.449
010	− 0.630	210	+ 9.370
011	− 0.709	211	+ 9.291
—	—	—	—
—	—	—	—
—	—	—	—
077	− 4.961	277	± 5.039
100	− 5.039	300	+ 4.961
101	− 5.118	301	+ 4.882
—	—	—	—
—	—	—	—
—	—	—	—
175	− 9.843	375	+ 0.157
176	− 9.921	376	+ 0.079
177	− 10.000	377	0.000

The row of nine lights at the bottom of the I/0 indicator panel is the binary input address indicator. It consists of bits 3 through 11 of the input address register. This address determines which one of the 504 syncoder circuit relays is closed. Each relay allows the analog output of syncoder to be sampled. These relays are physically located on the syncoder boards. The bays are wired in such a maner that each relay effectively lies at a junction point of an 8 by 64 matrix. The logic used to convert this binary address into a single relay closure is similar to that used for the output address decoding. Bits 3, 4 and 5 are decoded into the a signal required to activate one of the 8 positive line drivers. Bits 6 through 11 are decoded into a signal required to activate one of the 64 negative line drivers. An 8 by 64 diode matrix with relay coils at all but 8 cross points is then used to permit the output of any one of the 504 synapse integrators in C^3 to be connected to the A-D converter. Table 3 decodes the binary input address indication (read in octal) into the syncoder physical location in the bays. The value of the analog signal sampled through the input matrix is converted by the A-D converter and the corresponding binary number is displayed by a row of 12 indicator lamps on the front panel of that unit. These binary numbers can be stored by the PDP-8S and recalled from memory under program control. Table 4 shows octal numbers resulting from some analog voltage input values.

Table 3. Syncoder Locations Related to Controller Input Addresses

INPUT ADDRESSES Negative (Bits 6-11)	Positive (Bits 3-5) 00	01	02	03	04	05	06	07
00	1A1	1C9	1E17	2A25	2D5	2F13	3B21	3E1
01	1A2	1C10	1E18	2A26	2D6	2F14	3B22	3E2
02	1A3	1C11	1E19	2A27	2D7	2F15	3B23	3E3
03	1A4	1C12	1E20	2A28	2D8	2F16	3B24	3E4
04	1A5	1C13	1E21	2B1	2D9	2F17	3B25	3E5
05	1A6	1C14	1E22	2B2	2D10	2F18	3B26	3E6
06	1A7	1C15	1E23	2B3	2D11	2F19	3B27	3E7
07	1A8	1C16	1E24	2B4	2D12	2F20	3B28	3E8
10	1A9	1C17	1E25	2B5	2D13	2F21	3C1	3E9
11	1A10	1C18	1E26	2B6	2D14	2F22	3C2	3E10
12	1A11	1C19	1E27	2B7	2D15	2F23	3C3	3E11
13	1A12	1C20	1E28	2B8	2D16	2F24	3C4	3E12
14	1A13	1C21	1F1	2B9	2D17	2F25	3C5	3E13
15	1A14	1C22	1F2	2B10	2D18	2F26	3C6	3E14
16	1A15	1C23	1F3	2B11	2D19	2F27	3C7	3E15
17	1A16	1C24	1F4	2B12	2D20	2F28	3C8	3E16
20	1A17	1C25	1F5	2B13	2D21	3A1	3C9	3E17
21	1A18	1C26	1F6	2B14	2D22	3A2	3C10	3E18
22	1A19	1C27	1F7	2B15	2D23	3A3	3C11	3E19
23	1A20	1C28	1F8	2B16	2D24	3A4	3C12	3E20
24	1A21	1D1	1F9	2B17	2D25	3A5	3C13	3E21
25	1A22	1D2	1F10	2B18	2D26	3A6	3C14	3E22
26	1A23	1D3	1F11	2B19	2D27	3A7	3C15	3E23
27	1A24	1D4	1F12	2B20	2D28	3A8	3C16	3E24
30	1A25	1D5	1F13	2B21	2E1	3A9	3C17	3E25
31	1A26	1D6	1F14	2B22	2E2	3A10	3C18	3E26
32	1A27	1D7	1F15	2B23	2E3	3A11	3C19	3E27
33	1A28	1D8	1F16	2B24	2E4	3A12	3C20	3E28
34	1B1	1D9	1F17	2B25	2E5	3A13	3C21	3F1
35	1B2	1D10	1F18	2B26	2E6	3A14	3C22	3F2
36	1B3	1D11	1F19	2B27	2E7	3A15	3C23	3F3
37	1B4	1D12	1F20	2B28	2E8	3A16	3C24	3F4

Table 3. Syncoder Locations Related to Controller Input Addresses (Continued)

INPUT ADDRESSES Negative (Bits 6-11)	Positive (Bits 3-5) 00	01	02	03	04	05	06	07
40	1B5	1D13	1F21	2C1	2E9	3A17	3C25	3F5
41	1B6	1D14	1F22	2C2	2E10	3A18	3C26	3F6
42	1B7	1D15	1F23	2C3	2E11	3A19	3C27	3F7
43	1B8	1D16	1F24	2C4	2E12	3A20	3C28	3F8
44	1B9	1D17	1F25	2C5	2E13	3A21	3D1	3F9
45	1B10	1D18	1F26	2C6	2E14	3A22	3D2	3F10
46	1B11	1D19	1F27	2C7	2E15	3A23	3D3	3F11
47	1B12	1D20	1F28	2C8	2E16	3A24	3D4	3F12
50	1B13	1D21	2A1	2C9	2E17	3A25	3D5	3F13
51	1B14	1D22	2A2	2C10	2E18	3A26	3D6	3F14
52	1B15	1D23	2A3	2C11	2E19	3A27	3D7	3F15
53	1B16	1D24	2A4	2C12	2E20	3A28	3D8	3F16
54	1B17	1D25	2A5	2C13	2E21	3B1	3D9	3F17
55	1B18	1D26	2A6	2C14	2E22	3B2	3D10	3E18
56	1B19	1D27	2A7	2C15	2E23	3B3	3D11	3F19
57	1B20	1D28	2A8	2C16	2E24	3B4	3D12	3F20
60	1B21	1E1	2A9	2C17	2E25	3B5	3D13	3F21
61	1B22	1E2	2A10	2C18	2E26	3B6	3D14	3F22
62	1B23	1E3	2A11	2C19	2E27	3B7	3D15	3F23
63	1B24	1E4	2A12	2C20	2E28	3B8	3D16	3F24
64	1B25	1E5	2A13	2C21	2F1	3B9	3D17	3F25
65	1B26	1E6	2A14	2C22	2F2	3B10	3D18	3F26
66	1B27	1E7	2A15	2C23	2F3	3B11	3D19	3F27
67	1B28	1E8	2A16	2C24	2F4	3B12	3D20	3F28
70	1C1	1E9	2A17	2C25	2F5	3B13	3D21	
71	1C2	1E10	2A18	2C26	2F6	3B14	3D22	
72	IC3	1E11	2A19	2C27	2F7	3B15	3D23	
73	1C4	1E12	2A20	2C28	2F8	3B16	3D24	
74	1C5	1E13	2A21	2D1	2F9	3B17	3D25	
75	1C6	1E14	2A22	2D2	2F10	3B18	3D26	
76	1C7	1E15	2A23	2D3	2F11	3B19	3D27	
77	1C8	1E16	2A24	2D4	2F12	3B20	3D28	

Table 4. Representative Analog-to-Digital Conversions for Syncoder Voltages

Voltage	*Octal Number*
+10	4000
+9	4314
+8	4632
+7	5146
+6	5462
+5	6000
+4	6314
+3	6632
+2	7146
+1	7462
0	0000
−1	0314
−2	0632
−3	1146
−4	1462
−5	2000
−6	2314
−7	2632
−8	3146
−9	3463
−10	3777

THE NETWORK BAYS

The C² System also consists of three large network bays labeled left to right, Bay 1, Bay 2, and Bay 3. The bays are identical except that the power supplies and power switches for all three are located in Bay 1.

Each bay has three basic external parts—a large red, white, green, and gray removable patch panel, a small black patch panel, and a neon light display, all mounted on the front face of a large pull-out drawer containing the circuit boards. The light display and the two patch panels in a given bay all correspond to the same set of syncoders.

THE LARGE PATCH PANELS

Each large patch panel has six sections, A through F, arranged as shown in Figure 6. Each section is identical to the one shown in Figure 7 and contains syncoder areas, sample-and-hold locations, inter-bay connection locations, and access to an extra operational amplifier.

SYNCODER AREAS

There are 28 syncoder areas in each section. On the patch panel, they look like the one drawn in Figure 8. They are arranged in four rows of six followed by a row of four. The syncoders are referenced by the following scheme- "Bay Number", "Section Letter", "Syncoder Number". The syncoders in each section are numbered sequentially, 1 though 28. For example, "2A6" refers to the sixth syncoder area (last one in the first row) of the A section in Bay 2.

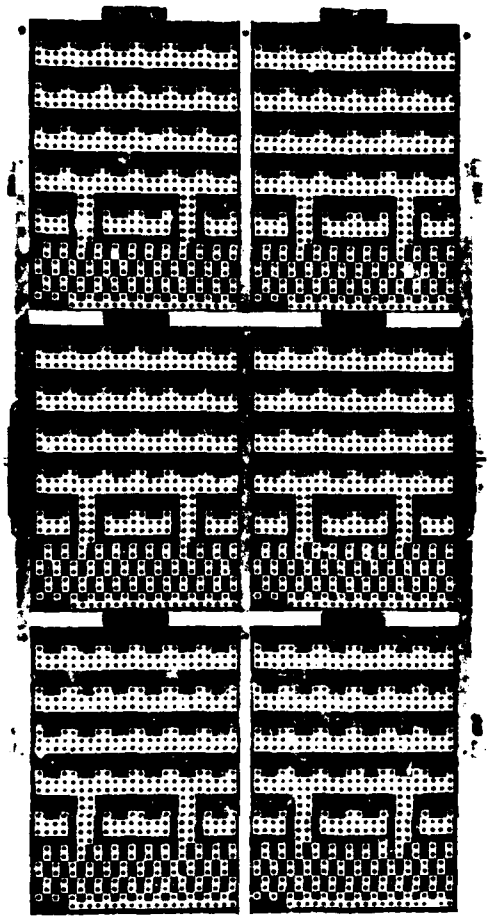


Figure 6. A Large Patch Panel

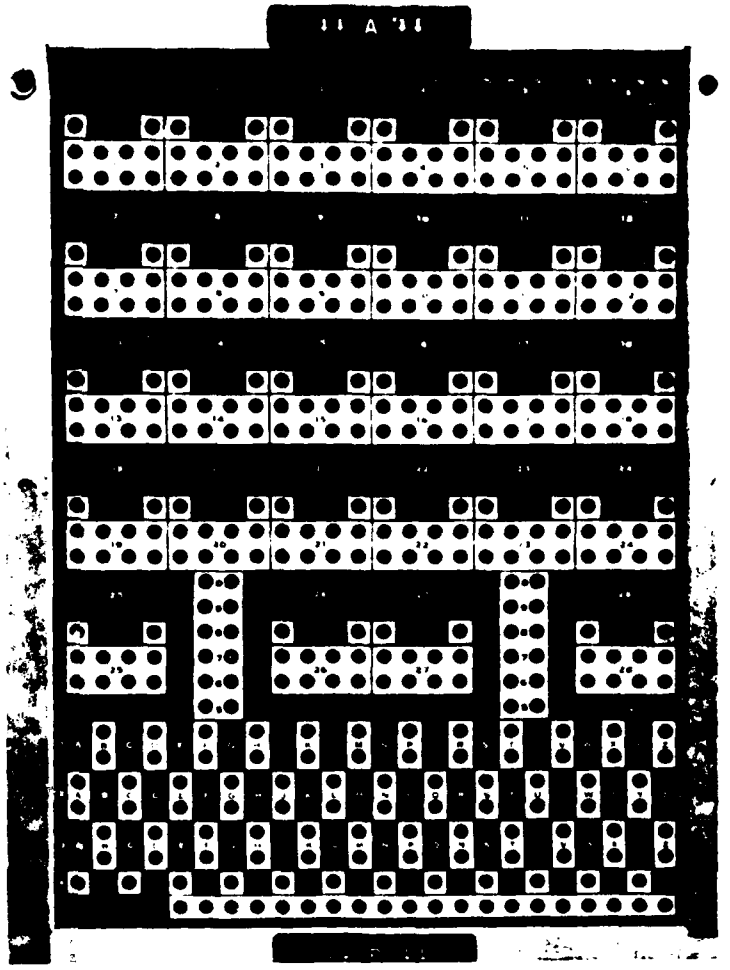


Figure 7. A Single Patch Panel Section

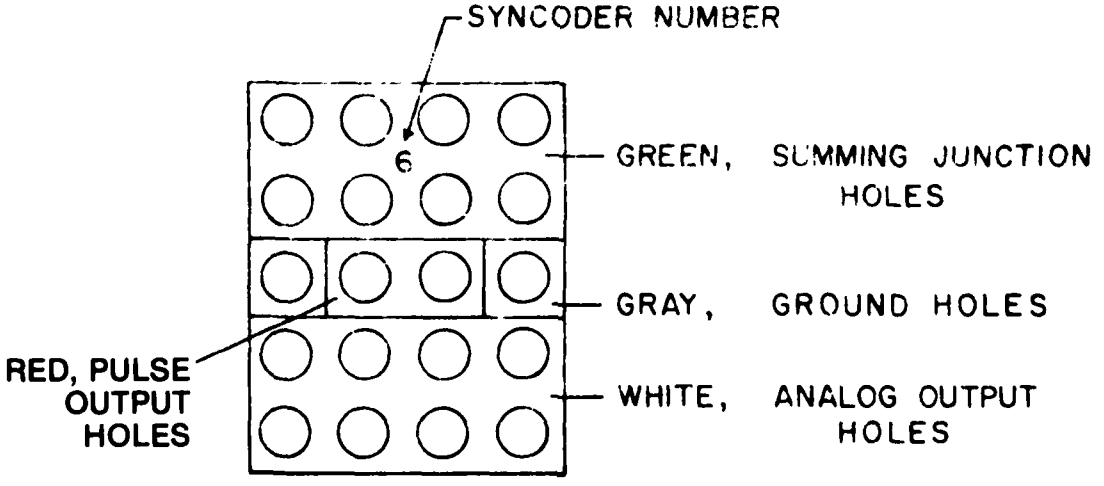


Figure 8. An Individual Syncoder Patch Panel Area

The green holes access the summing junction of the initial amplifier stage. The white holes are wired to the output of the synapse section (an analog signal), which is also the input to the encoder section, while the red holes are the termination of the (pulse) output signal from the encoder section. The gray holes are tied to the system ground.

SAMPLE-AND-HOLD LOCATIONS

The seven rows of alternating green and white holes just below the 28 syncoders are assigned to sample-and-hold circuits. A PDP-8 program, SYNSET, with teletype input can provide voltages to be stored on these sample-and-hold boards. These sample-and-hold locations can be patched to the summing junction of any syncoder to supply a fixed voltage as a bias voltage or a weighting voltage for a pulse train. The scheme for referencing the sample-and-hold locations is described here and shown in Figure 9. Each vertical pair of dots has a row number (one through three) in the left hand edge of the row. Row 4 has a single row of holes. Each of the 24 positions along the row has a letter assigned to it ("A" through "Z", with "I" and "O" omitted). Each location (vertical pair) may be referenced as follows - "Bay Number", "Section Letter", "Row Number", and "Letter". For example, 2A1C refers to Bay 2, Section A, first row, third vertical pair. In this area the two different colors (white and green) serve only to discriminate one sample-and-hold location from its adjacent neighbors.

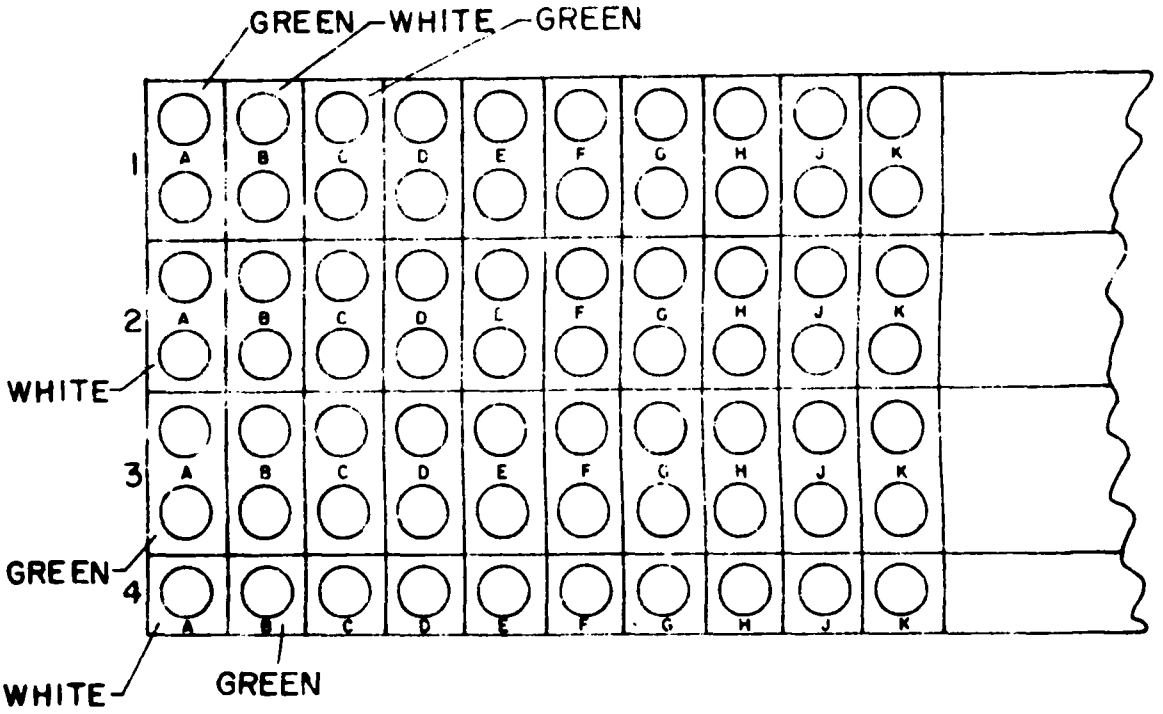
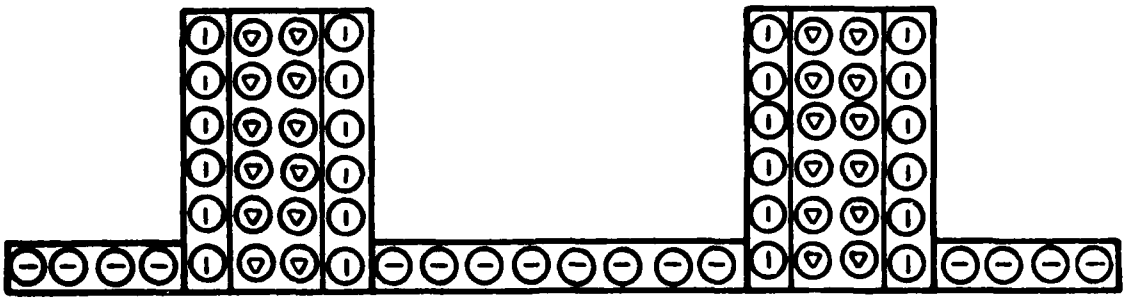


Figure 9. A Portion of the Sample-and-Hold Locations Area

INTER-BAY CONNECTION LOCATIONS

In between the syncoder and sample-and-hold areas are the inter-bay connection locations shown in Figure 10. All the red holes are wired to jacks on the back of each bay, with portions of two different jacks connected to each section. The two subareas are differentiated on the patch panel as a set of 24 "vertical" holes (4 columns of 6 holes) and 16 "horizontal" holes (4 groups of 4). The gray holes are system ground connections, which can be easily paired with the vertical holes using dual patch-panel plugs.

All the inter-bay connection locations (red holes) from the large patch panel terminate in five 50-pin jacks, although only 48 pins are used on each connector. The 48 vertically arrayed red holes in sections A and D in each bay are wired to J10 on the back of the bay. J10 is also hardwired to the small patch panel as described in the next section. The 48 vertical red holes in sections B and E are wired to J11 and those in sections C and F are wired to J12. The 48 horizontal red holes in sections A, D and B are wired to J13 and those in sections E, C and F to J14. Table 5 contains the above information in tabular form. Cables are used to connect one jack to any other Jack on any bay (including another jack on the same bay). This is the primary way in which the bays a communicate with each other.



INTER-BAY CONNECTION HOLES:

⊖ "HORIZONTAL" — GROUP HOLES

① "VERTICAL" — GROUP HOLES

⊙ SYSTEM GROUND HOLES

Figure 10. A Representative Inter-Bay Connection Locations Area

Table 5. Inter-Bay Connections

Type	Section	Jack Number
Vertical	A, D	J10*
Vertical	B, E	J11
Vertical	C, F	J12
Horizontal	A, D, B	J13
Horizontal	E, C, F	J14

*Also hardwired to the small (black) patch panel

EXTRA OPERATIONAL AMPLIFIER AREA

The bottom row of holes in each section accesses an extra operational amplifier (op amp), which can be used for increasing the fan-out capability of a selected syncoder output or for general analog signal processing. As with the syncoder areas, the green holes are the summing junction input, and the white holes are connected to the op amp output.

THE SMALL PATCH PANELS

On the left-hand side of each bay, below the large patch panel, is a small black patch panel. It is not removable, but accepts the same type connectors as the large patch panel. As can be seen in Figure 11, it has only three types of holes: syncoder pulse outputs, extra operational amplifier summing junction inputs, and a limited set of inter-bay connection holes.

SYNCODER PULSE OUTPUT HOLES

The small patch panel provides the pulse output of each syncoder for monitoring. The top portion (rows A through Q) is arranged like a miniature version of the large patch panel. One hole corresponds to the pulse output of each syncoder. Holes 2, 5, 8, and 11 in rows E, K, and Q, which correspond to the inter-bay connection locations area on the large patch panel, are not pulse output holes.

EXTRA OPERATIONAL AMPLIFIER SUMMING JUNCTION INPUT HOLES

Holes 2, 5, 8, and 11 in rows E, K, and Q provide 2 more inputs to the summing junction of the extra operational amplifier for each section. These holes are designated with an "X" in Figure 11.

INTER-BAY CONNECTION HOLES

Rows R through W are wired to inter-bay connection jacks on the back of the bay. Columns 1, 2, 3 and 12 are connected to J9. These 24 pins, specified in Figure 11, are the only pins of J9 in use. Columns 4 through 11 are connected both to J10 and also to the "vertical" inter-bay connection holes in sections A and D of the large patch panel, as discussed earlier.

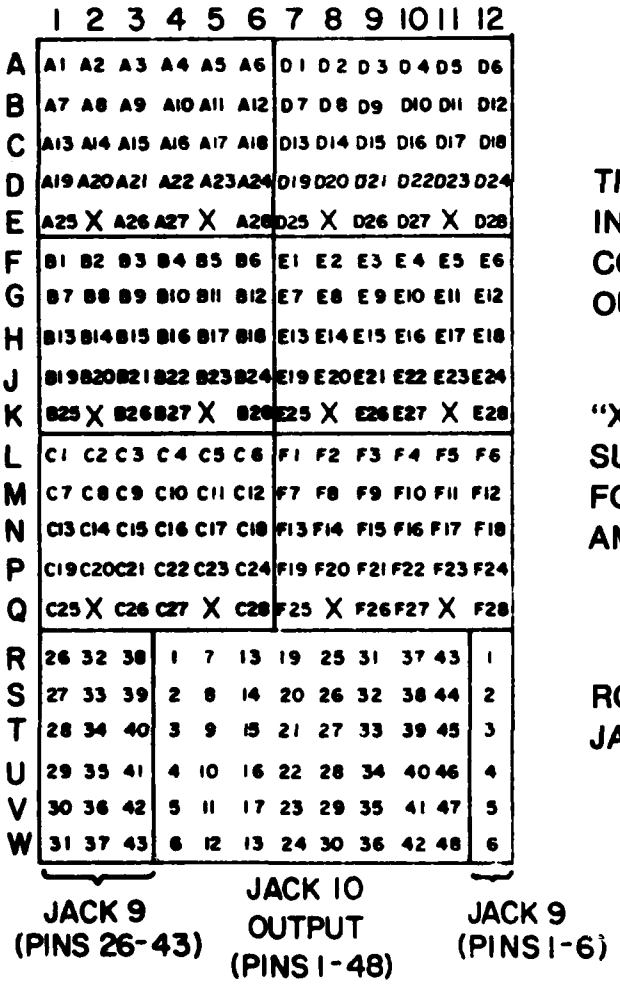


Figure 11. The Small Patch Panel

NEON LIGHT DISPLAY PANELS

The neon light display panel, located just below the large patch panel on each bay, has a single neon light to represent the pulse output of each syncoder (1 through 28) in each section (A through F). The lights, represented by circles in Figure 12, are arranged in the same order as are the syncoder areas on the large patch panel.

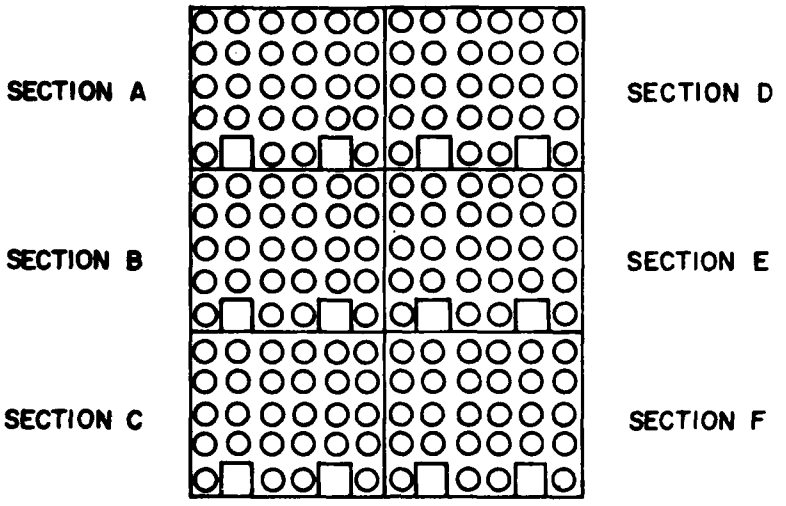


Figure 12. The Neon Light Display Panel

CARD FILE RACKS

As mentioned earlier, the patch panels of each bay are actually mounted on the front of a large pull-out drawer featuring two hinged frames (one on each side), each containing seven rows of card mounting racks. (Each of the card file rows has slots for 17 circuit boards except rows A, B, C, D, E, and F of bay 1, which have 16 slots.) Most of the circuits of the C^2 System are on circuit boards which are inserted in these card file racks. Figure 13 shows a front view of a bay with the drawer pulled out and the card file doors opened.

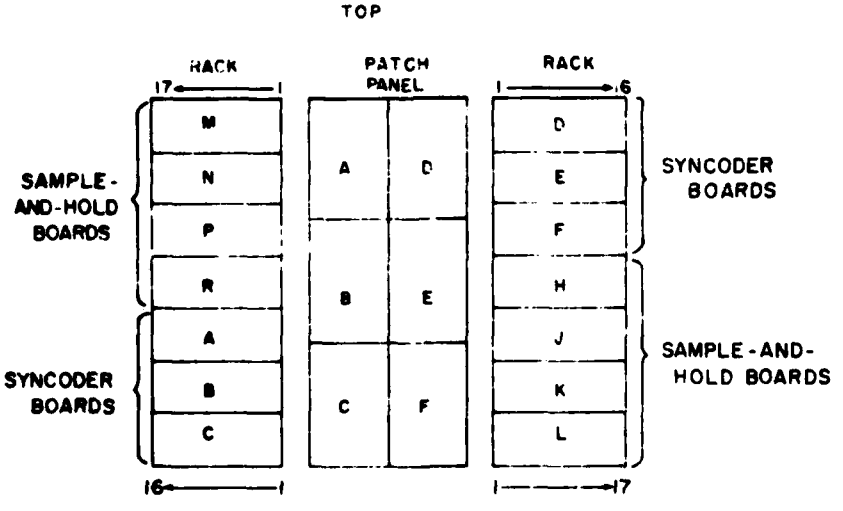


Figure 13. General Location of the Card Racks

THE C² SYNCODER CIRCUITS

At the time of this writing, there are five circuit implementations of the syncoder principles in use with the C² syncoder network simulator. The five versions, called Mod 1 through Mod 5 respectively, represent a continuing engineering development effort aimed at increasing performance and reducing cost. This section brings together in a single concise reference all operation and maintenance data available on these circuits. Although the Mod 1 and Mod 2 boards were described by Gruenke and Mundie (1968), their descriptions are repeated here for completeness.

For each circuit, there is a circuit diagram, a parts list, labled photographs showing both sides of the board, a commentary on circuit function, and a step-by-step checkout procedure which can be used for maintenance purposes. At the end of this section is a listing of the significant information processing features of each design. This permits a C² programmer to pick that version of the syncoder implementation which bests suits the information processing task at any point in an arbitrary syncoder network.

Each syncoder circuit board contains two circuits, identified as A and B. (Circuit A occupies the left half of the board looking at the component side with the connector at the bottom.) Thus, each syncoder location on a front panel corresponds to one half of a syncoder circuit board, and the boards for the 28 syncoders in each section of a patch panel are located in the first 14 slots of the correspondingly lettered card file row. Figures 14 and 15 show the relationship between patch panel locations and card file locations for a representative section from each half of a bay.

ALL PATCH PANEL SECTIONS (A—F)

BOARD No.

CIRCUIT DESIGNATION

1 A 1	1 B 2	2 A 3	2 B 4	3 A 5	3 B 6
4 A 7	4 B 8	5 A 9	5 B 10	6 A 11	6 B 12
7 A 13	7 B 14	8 A 15	8 B 16	9 A 17	9 B 18
10 A 19	10 B 20	11 A 21	11 B 22	12 A 23	12 B 24
13 A 25		13 B 26	14 A 27		14 B 28

SYNCODER No.

Figure 14. Syncoder Circuit Identifications as a Function of Patch Panel Location

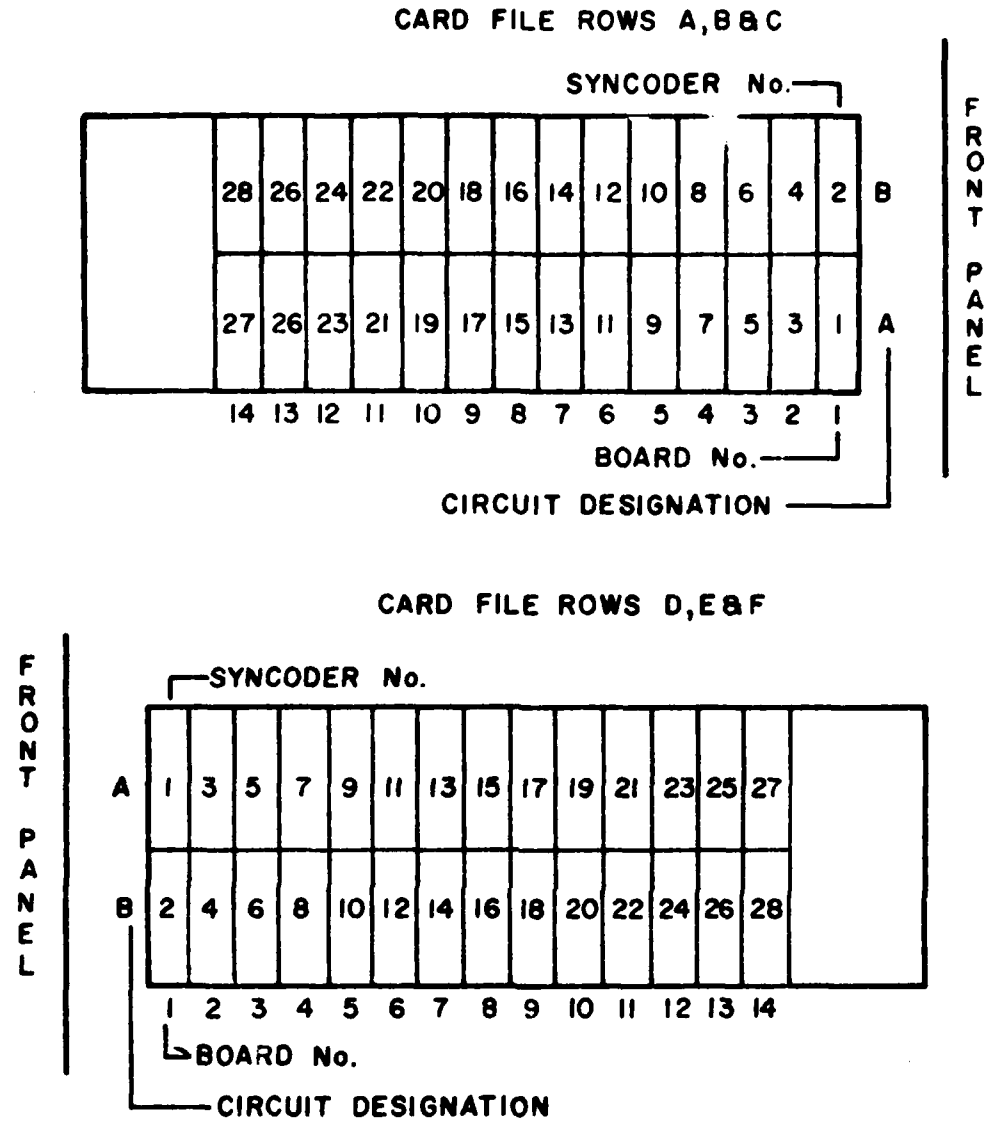


Figure 15. Syncoder Numbers Related to Card File Locations

The schematics show only one syncoder circuit, rather than showing two identical circuits. However, power supply bypass capacitors which serve both circuits are shown on the schematic even though they do not occur twice on the board. In the text describing each syncoder, reference is made to input/output pins for the circuit located on the left half of the board (components with an A suffix in layout diagrams). For example, the ± 12-volt pulse output will be referred to as pin J, with the implicit understanding that if the circuit on the right half of the board were under consideration, its pulse output is found on pin L as is clearly shown on the schematic.

MOD 1 SYNCODER

CIRCUIT DESCRIPTION

The Mod 1 Syncoder was developed directly from the syncoder circuits used in the Root C syncoder network simulator described by Gruenke and Mundie (1968). The circuit is shown in Figure 16; the circuit board layout is shown in Figures 17 and 18; and the list of components is given in Table 6. The operational amplifier, OA1, is used as a low-pass filter to permit summing the inputs from any combination of up to eight synapse button and analog signal sources. The feedback capacitor, C1, can be made larger by plugging an additional capacitor into the program patch panel, thereby controlling the pass band of the filter. The output of the operational amplifier, S(t), therefore simulates the spatial and temporal summated potential difference thought to be the physiologically

significant analog signal encoded by a neuron. This signal is available to the program patch panel through pin C, and may be used as an analog input signal to any syncoder, or as a weighting voltage for any synapse button. Pin E is connected to a bus which permits the PDP-8S computer to select any syncoder in C^3, close the appropriate relay (K1), and sample the value of S(t) through the A-D converter. Diode D1 protects the relay drivers from inductive transients when the switching transistors turn off.

The encoding section of the Mod 1 board generates output pulses whenever the amplitude of S(t) exceeds the amplitude of an exponentially decaying threshold voltage which is developed across capacitor C5. Q2 and Q5 are connected as a conventional collector-coupled monostable multivibrator. In the quiescent state, Q2 is off and Q5 is conducting so the emitter of Q4 is below ground cutting off Q1 and Q6. The threshold voltage, T(t), stored on C5 keeps the base of Q3 negative while C5 discharges through R13, D3, and Q5 towards zero volts with a time constant of (R13)•(C5). Q3 serves as an emitter follower and as a level shifter which adds one p-n junction voltage drop to T(t) and provides an impedance buffer so that the negative voltage T(t) may be compared with the positive voltage S(t) at the base of Q2. R3, R6, and R9 form a voltage divider such that when S(t) is more positive than T(t) is negative, Q2 is turned on. Note that the Q3 base emitter junction compensates for the Q2 base emitter junction offset so that the comparison may be carried out accurately. R16 and R7 serve to permit DC offset adjustment and thereby set the exact triggering level. However, offset voltage drift variations is not compensated with this circuit. Q2 turns on regeneratively when it is triggered: its collector voltage starts to fall causing Q5 to be driven into cutoff through C4; therefore the Q5 collector voltage rises, producing regenerative positive feedback through C5 and D2 to insure that Q2 turns on completely. Thus ends the quiescent state.

During the active state, Q2 is on and Q5 is off. C5 charges through R11, D2, and Q2 with a time constant of (R11)•(C5), keeping Q2 in saturation. Once C5 is completely charged to + 12 volts, Q2 is kept turned on by base current supplied through R9 and D2 until the end of the active state. Because Q1 is saturated and R6 shunts the base of Q2, Q2 may or may not be saturated depending upon the setting of R16. While Q5 is off, R14 holds the base of Q4 near + 12 volts so that D3 is reverse biased while C5 is charging. The emitter of Q4 remains high during the active state, causing Q1 and Q6 to saturate. Q1 shunts all current generated by a positive value of S(t) to ground preventing S(t) from biasing Q2 into conduction through R3. Thus, S(t) can not retrigger the one shot during the encoder active state. This corresponds to the absolute refractory period of a neuron when an input signal, no matter how large, can not trigger a regenerative pulse. The duration of the active state is controlled by the discharge time constant of the voltage across C4 which keeps Q5 cut off. C4 charges toward zero volts through R10 and Q2 with a time constant of (R10)•(C4). When the voltage at the base of Q5 exceeds the base emitter voltage drop, Q5 turns on and the circuit regeneratively returns to its quiescent state. At the end of the regenerative cycle, the base of Q4 is near ground and the emitter of Q4 is slightly below ground, insuring that both Q1 and Q6 are completely cut off. With Q1 cut off, S(t) is again applied to the base of Q2 through R3 and R6 and is continuously compared with T(t) which is applied to the base of Q2 through R9. Thus ends the active state.

The encoder has two outputs, a zero to 12-volt pulse output on pin H and a − 12 to 12 volt pulse on pin J. The zero to 12-volt output on pin H is taken from the emitter of Q4 and has already been described in detail. It is used in C^3 to drive a neon lamp driver circuit which flashes a neon lamp each time the syncoder generates a pulse. The ± 12-volt output from pin J is brought out to the program patch panel for use in driving the synapse buttons required by networks of syncoders. It is generated by transistors Q6 through Q9 from the 12 volt pulse at the emitter of Q4. During the encoder quiescent state, Q6 is cut off, causing Q7 and Q8 to be cut off and Q9 to be saturated. Thus, the output voltage is held near − 12 volts. R21 and R22 provide short circuit protection for Q9. During the encoder active state, Q6 is saturated, causing Q7 and Q8 to saturate while causing Q9 to be cut off. Thus the output voltage is held near 12 volts. R19 serves to protect Q8 from short circuits, but a potential failure mode exists for Q7 which is not protected from external short circuits except by a limited base drive through R20. It could self-destruct under thermal runaway conditions, but this has not been observed in more than 4 years of system operation.

CHECKOUT PROCEDURE

1. Ground the summing junction of the op amp, OA1, (pin B) through a 100 kΩ resistor. Adjust R2, to zero the output voltage at pin C, within ± 5 mV.
2. Apply a 2 Vp-p, 1 kHz sine wave to the summing junction (pin B) of OA1 through a 100 kΩ resistor. Verify that the output of op amp (pin C) has an inverted sine wave of the same magnitude. This confirms operation of the op amp.
3. Close relay K1 and observe inverted since wave again, this time at pin E. This verifies operation of D1 and K1.
4. Vary amplitude of sine wave, while monitoring the zero to 12-V pulse output of encoder on pin H. Does the output interval exhibit phase locking at integer multiples of 1 with shorter intervals corresponding to larger input amplitude? If so, this verifies operation of the encoder (Q2, Q4, Q5).
5. Observe the ± 12-V pulse output on pin J. It should track with the encoder pulse output from pin H as the amplitude of the input sine wave is varied? Apply a 1 kΩ load from pin J to ground. If the output pulse height still greater than + 8 V and the resting level less than − 8 V, this verifies operation of the output stage (Q6, Q7, Q8, and Q9).

6. Ground pin B through a 100 kΩ resistor again, and apply an inhibitory voltage to the encoder circuit on the other side of the board under test, Adjust R16 to verify that the encoder can be turned on or off by R16. Adjust so that the encoder is firing at an interval greater than 30 ms. This serves to zero the encoding threshold offset voltage.

7. Apply a negative input voltage to pin B through a 100 kΩ resistor so that the encoder output free runs at some convenient rate. Use an oscilloscope probe to verify that Q1 saturates during each output pulse. Verify that the emitter of Q3 starts at − 11 V at the end of each output pulse. This completes the checkout of the Mod 1 board.

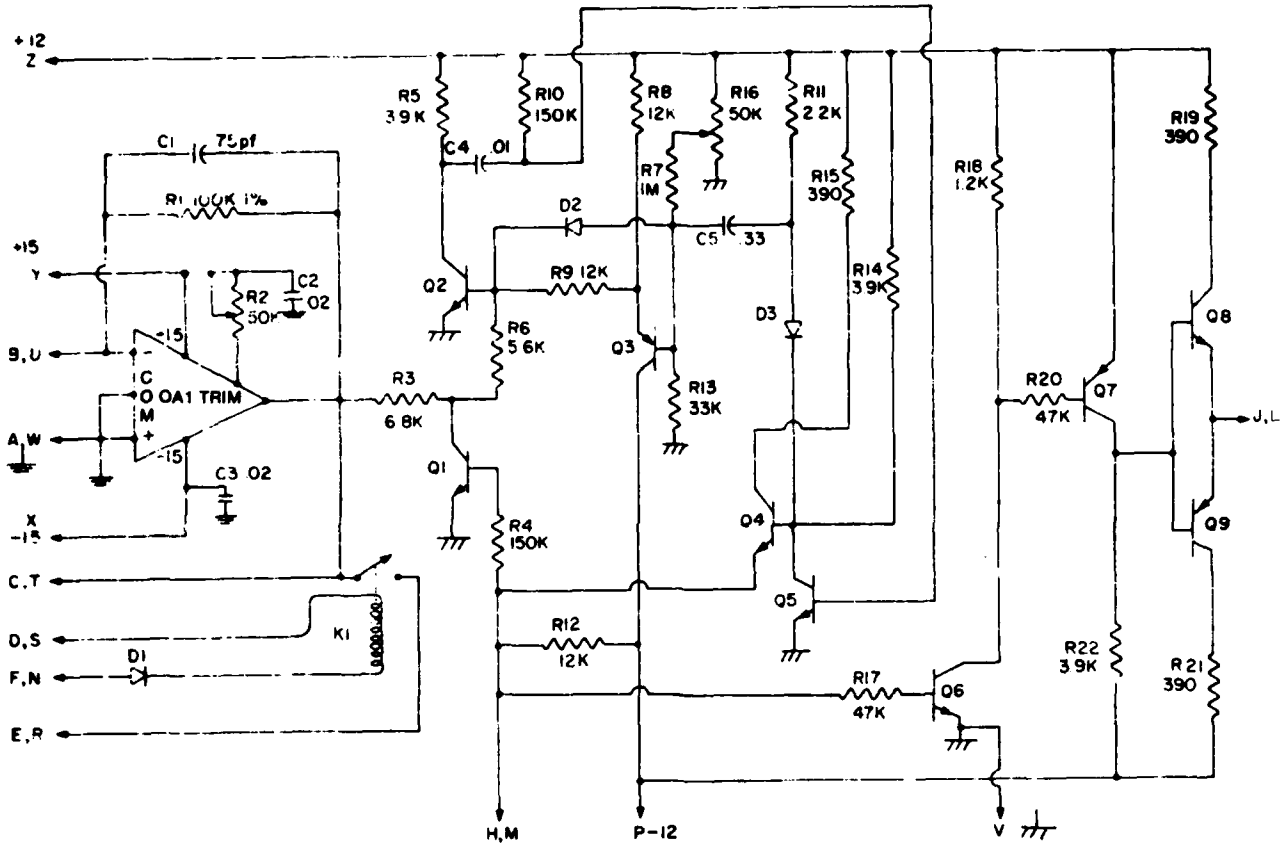


Figure 16. Mod 1 Syncoder Circuit

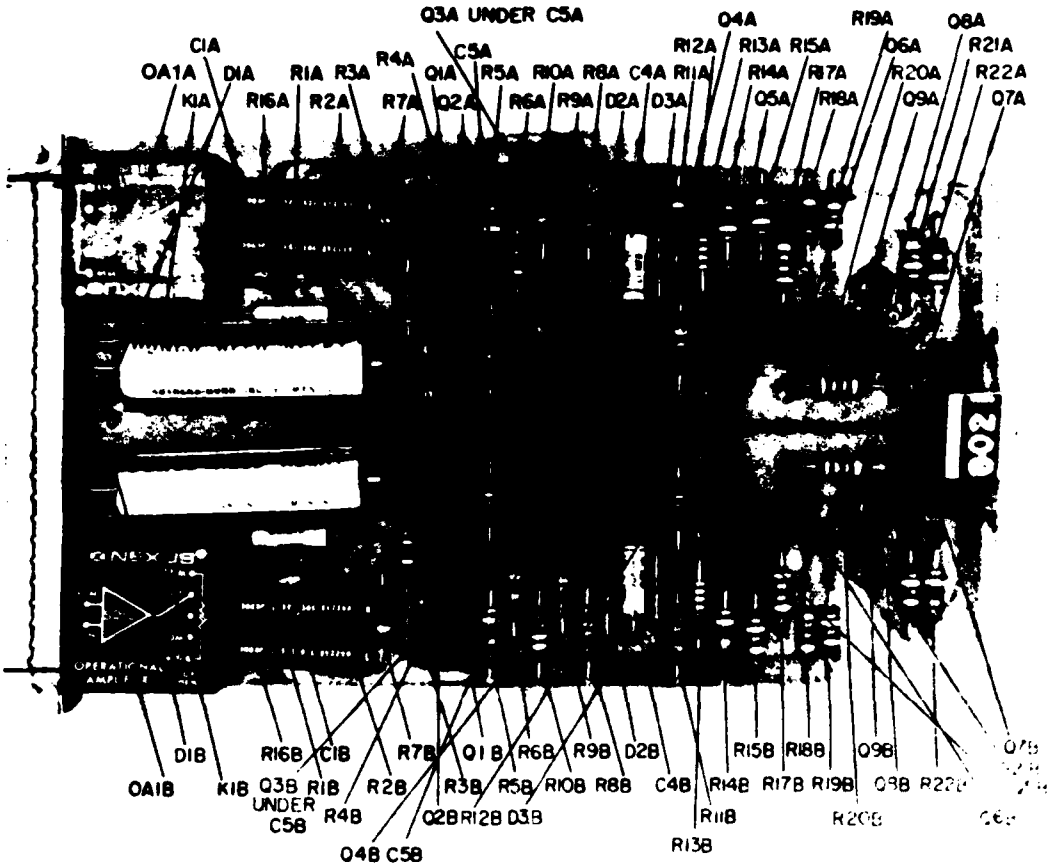


Figure 17. Mod 1 Syncoder Board (component side)

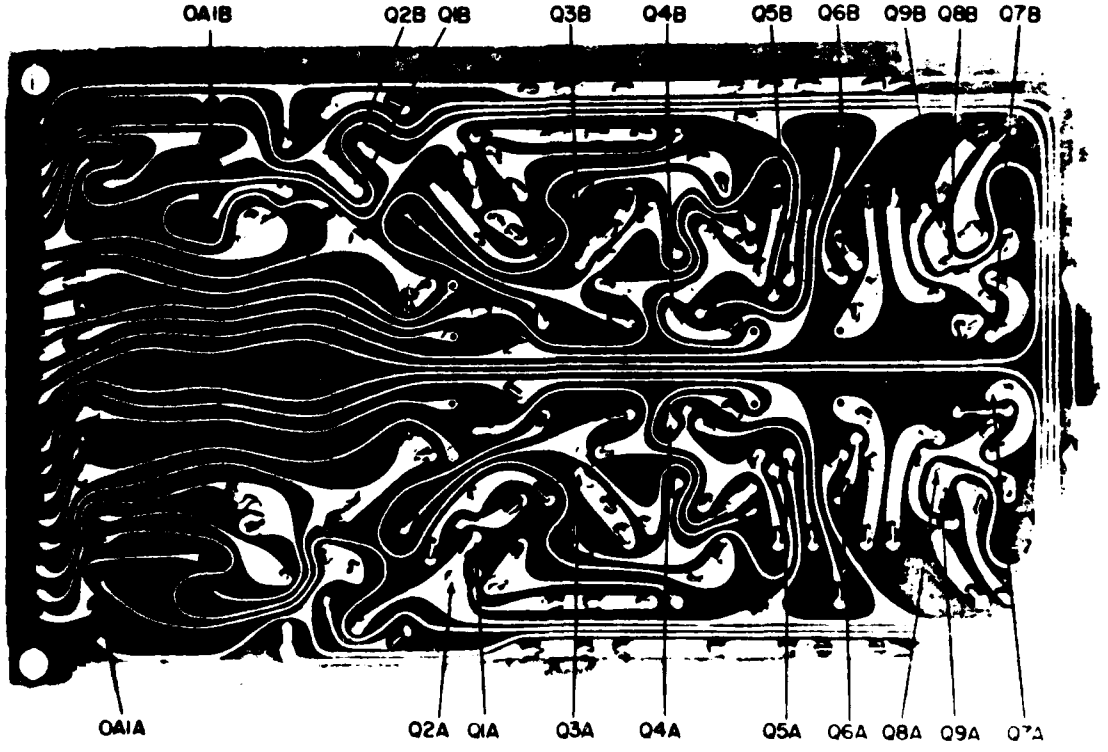


Figure 18. Mod 1 Syncoder Board (foil side)

Table 6. Components for the Mod 1 Syncoder Circuit

Designation	Description
C1	75 pF ceramic capacitor
C2,3	.02 μF ceramic capacitor
C4	.01 μF mylar capacitor
C5	.33 μF mylar capacitor
D1,2,3	1N4154 diode
K1	Struthers-Dunn RR1A reed relay
OA1	Nexus SQ-10 operational amplifier
Q1,2,4,5,6,8	2N3566 NPN transistor
Q3,7,9	2N3638 PNP transistor
R1	100 kΩ , 1/2 W, 1% film resistor
R2,16	50 kΩ Bourns 3068P-1-503 potentiometer
R3	6.8 kΩ resistor
R4,10	150 kΩ resistor
R5,14,22	3.9 kΩ resistor
R6	5.6 kΩ resistor
R7	1 MΩ resistor
R8,9,12	12 kΩ resistor
R11	2.2 kΩ resistor
R13	33 kΩ resistor
R15,19,21	390 Ω resistor
R17,20	47 kΩ resistor
R18	1.2 kΩ resistor

Note: All resistors are 1/2 watt, 10% tolerance unless otherwise specified.

MOD 2 SYNCODER

CIRCUIT DESCRIPTION

The Mod 2 Syncoder schematic, shown in Figure 19, is the same as that used for Mod 1. There is a slight difference in the physical layout of components between the two boards, and a different manufacturer supplied the operational amplifier. The Mod 2 circuit board is shown in Figures 20 & 21, and the corresponding list of components is given in Table 7. Since the circuit function is exactly the same as for the Mod 1 circuit, a detailed description is not repeated here.

CHECKOUT PROCEDURE

The Mod 2 checkout procedure is identical to the Mod 1 checkout procedure.

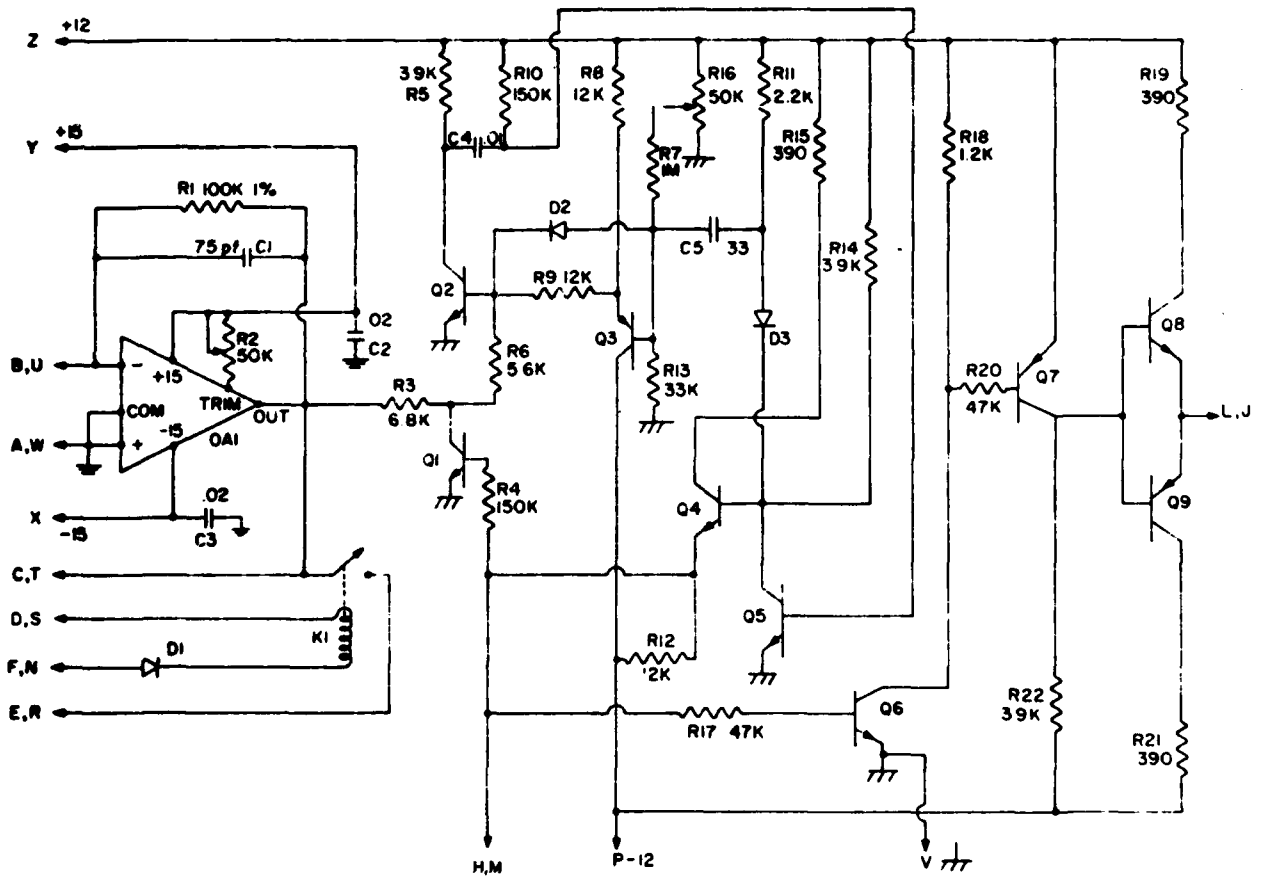


Figure 19. Mod 2 Syncoder Circuit

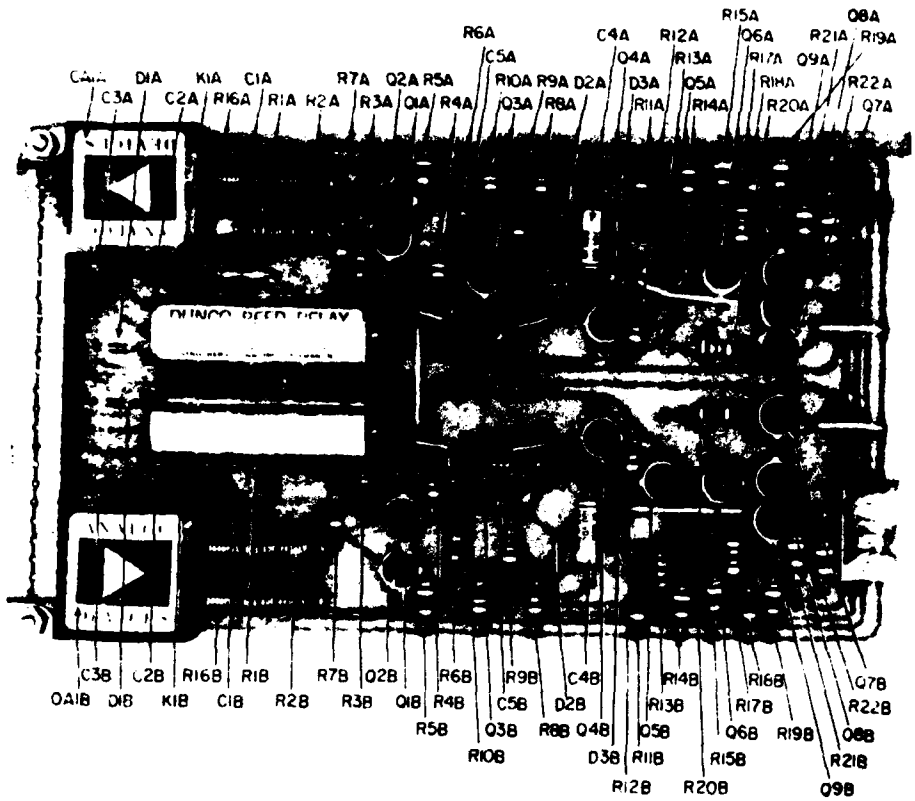


Figure 20. Mod 2 Syncoder Board (component side)

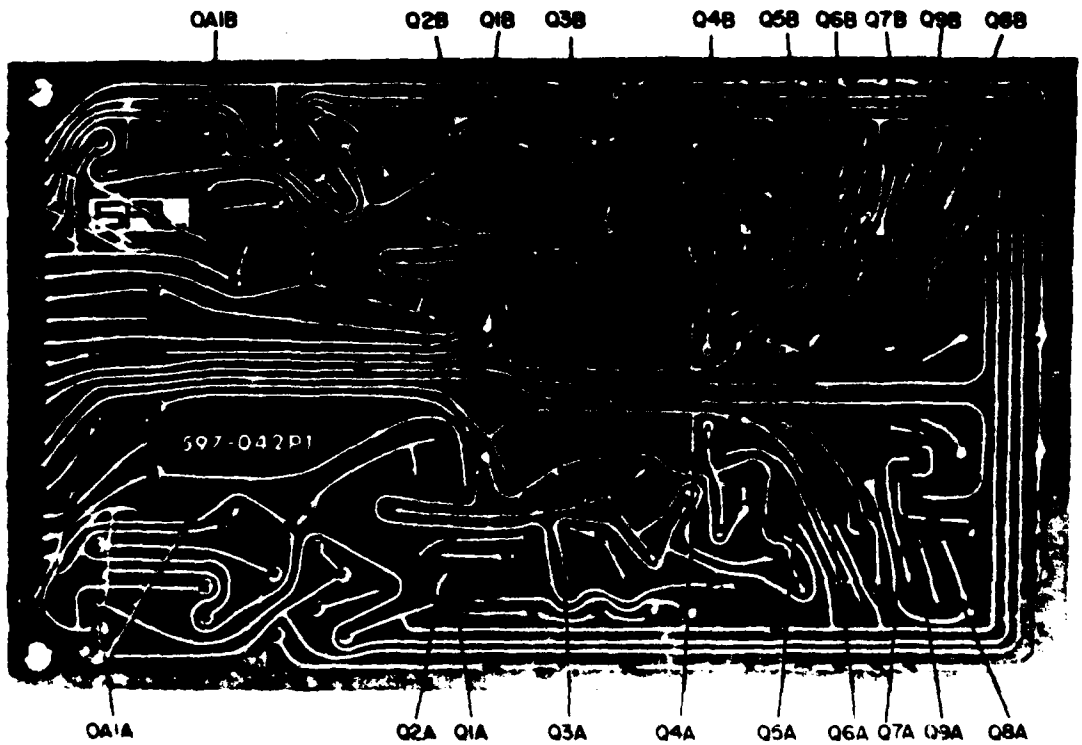


Figure 21. Mod 2 Syncoder Board (foil side)

Table 7. Components for the Mod 2 Syncoder Circuit

Designation	Description
C1	75 pF ceramic capacitor
C2,3	.02 μF ceramic capacitor
C4	.01 μF mylar capacitor
C5	.33 μF mylar capacitor
D1,2,3	1N4154 diode
K1	Struthers-Dunn RR1A reed relay
OA1	Analog Devices 1055 operational amplifier
Q1,2,4,5,6,8	2N3566 NPN transistor
Q3,7,9	2N3638 PNP transistor
R1	100 kΩ , 1/2 W, 1% film resistor
R2,16	50 kΩ Bourns 3068P-1-503 potentiometer
R3	6.8 kΩ resistor
R4,10	150 kΩ resistor
R5,14,22	3.9 kΩ resistor
R6	5.6 kΩ resistor
R7	1 MΩ resistor
R8,9,12	12 kΩ resistor
R11	2.2 kΩ resistor
R13	33 kΩ resistor
R15,19,21	390 Ω resistor
R17,20	47 kΩ resistor
R18	1.2 kΩ resistor

Note: All resistors are 1/2 watt, 10% tolerance unless otherwise specified.

MOD 3 SYNCODER

CIRCUIT DESCRIPTION

The design goal for the Mod 3 Syncoder was to make the minimum necessary and sufficient modifications to the Mod 2 circuit which would permit independent variation of both the output pulse width and the encoding threshold time constant. The Mod 3 circuit schematic is shown in Figure 22; the board layout is shown in Figures 23 & 24; and the components are listed in Table 8. As mentioned under the circuit description of the Mod 1 syncoder, the discharge time constant of C4 controls the output width, and the discharge time constant of C5 is equal to the encoding threshold time constant.

At first look, the obvious modification is to change the value of C4 and C5. Unfortunately, the circuit fails to operate as expected when the ratio of C5 to C4 is varied from its original design value of 33 to 1. If C4 is increased to reduce this ratio, there is no proportional increase in output pulse width. The reason is that once C5 has completed its charging cycle during the active state, there is not enough bias current supplied through R10 and D2 to keep Q2 in saturation. As Q2 comes out of saturation, its rising collector voltage is coupled through C4 to initiate the regenerative turn off which should not have occurred until C4 discharged all the way to zero volts. By adding a transistor and two resistors to supply base bias current to Q2 during the active state of the encoder, it becomes possible for C4 to fully discharge before the regenerative turn off cycle is triggered.

The major difference between the schematic for the Mod 2 board and the schematic for the Mod 3 board is the addition of transistor Q10 and resistors R23 and R24 in the Mod 3 circuit. All other components remain unchanged, except that the inexpensive 741 integrated circuit operational amplifier was used in fabrication of the Mod 3 board, rather than the more expensive encapsulated op amp used in the Mod 2 board.

A brief description of the circuit operation is included here for the benefit of the reader who may be interested in the Mod 3 circuit. The 741 integrated circuit operational amplifier, IC1, performs the summing and low-pass filtering function required to generate the analog signal, S(t), used as the input to the encoder and as an output of pin C. The feedback resistor R1 and capacitor C1 are mounted in plugs to facilitate changing the filter response. Q2 and Q5 form a collector-coupled multivibrator in which Q2 is off and Q5 is on during the quiescent state, and Q3 serves as an emitter follower to couple the threshold voltage, T(t), to te base of Q2 through R9. Whenever S(t) reaches a positive voltage level where it can supply more current through R3 and R6 to the base of Q2 than T(t) at the emitter of Q3 can sink through R9, then Q2 is turned on. That causes the regenerative turn-off of Q5. During the active state, C4 discharges through R10 and Q2 while C5 charges through R11, D2, and Q2. For proper operation of the Mod 3 circuit, it is necessary that (R10)•(C4) be larger than (R11)•(C5) so that C5 is always fully charged to 12 volts at the end of every pulse. If (R11)•(C5) is very much smaller than (R10)•(C4), then transistor Q10 is biased on through R24 and supplies the base current through R23 to keep Q2 in saturation until C4 fully discharges. At that point, base bias current through R10 triggers Q5 on and regeneratively returns Q2 and Q5 to the quiescent state, ending the active state.

Note that during the active state, the collector of Q5 is high causing Q1 and Q10 to be saturated and Q4 to be high. When Q4 is high, Q6, Q7, and Q8 are saturated and the output at pin J is high. In the quiscent state, the collector of Q5 is low, causing Q1 and Q10 to be cut off and Q4 to be low. Since Q4 is low, Q6, Q7, and Q8 are cut off and Q9 is saturated so that the output at pin J is low.

CHECKOUT PROCEDURE

The Mod 3 checkout procedure is almost identical to the Mod 1 checkout procedure and is not repeated here. The only difference is that if R16 is unable to turn the encoder off with the input grounded, then Q10 may have a collector emitter short.

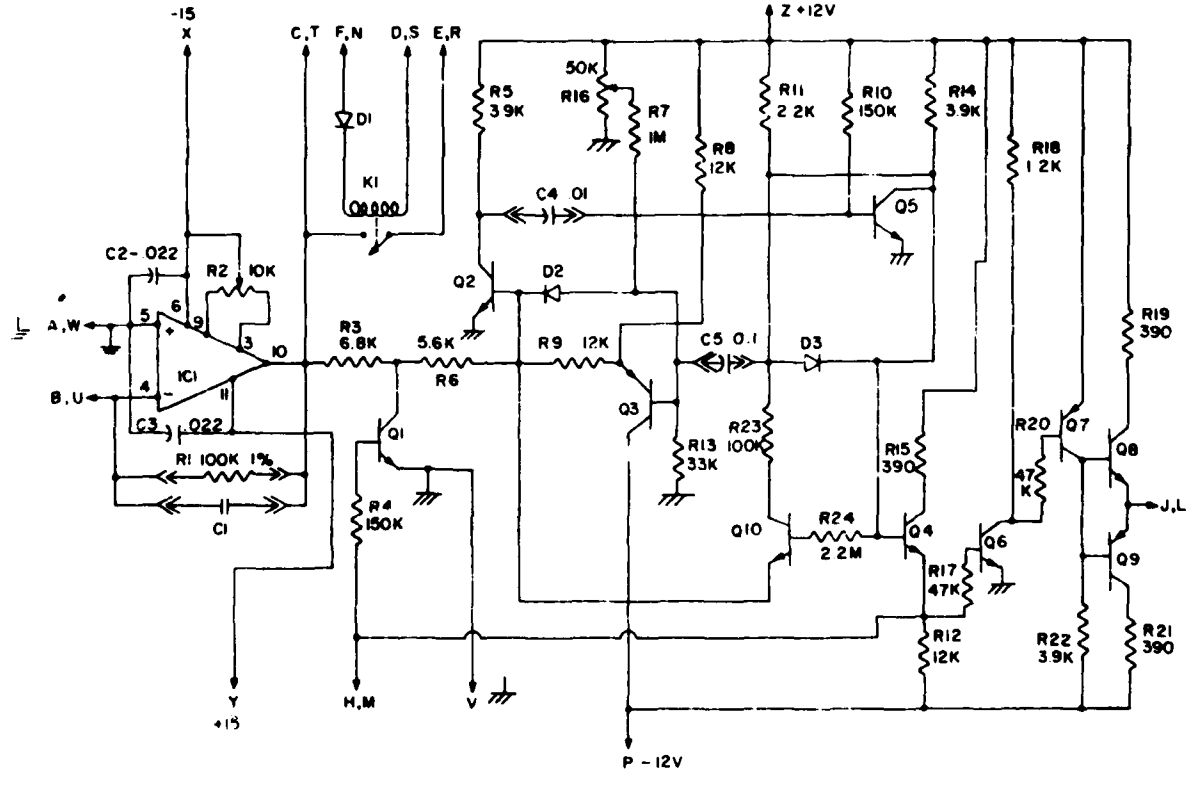


Figure 22. Mod 3 Syncoder Circuit

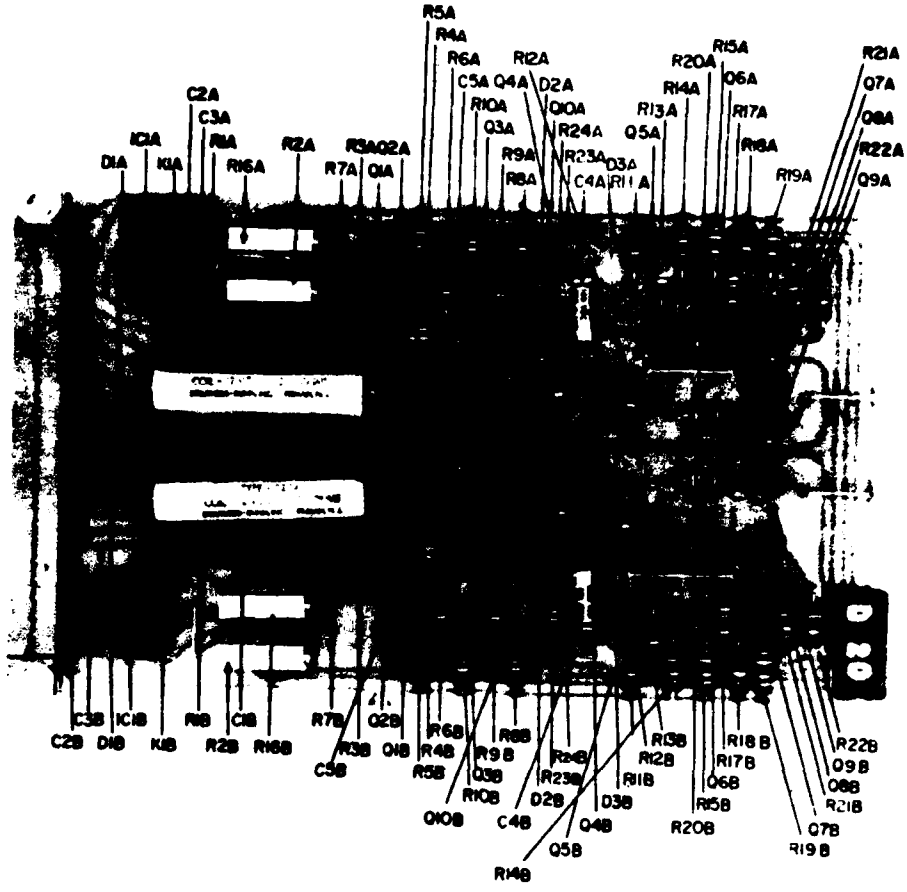


Figure 23. Mod 3 Syncoder Board (component side)

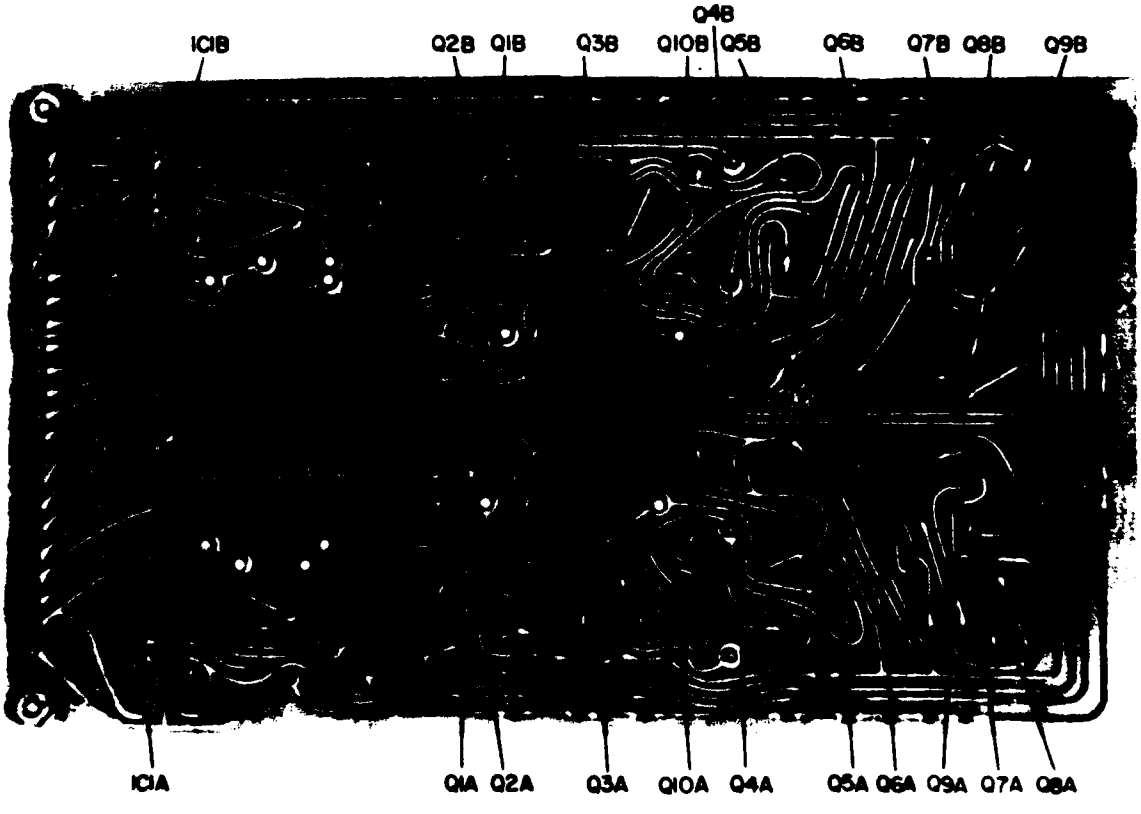


Figure 24. Mod 3 Syncoder Board (foil side)

Table 8. Components for the Mod 3 Syncoder Circuit

Designation	Description
C1	75 pF ceramic capacitor
C2,3	.022 μF ceramic capacitor
C4	.01 μF mylar capacitor
C5	.068 μF mylar capacitor
D1,2,3	1N4154 diode
IC1	741 operational amplifier
K1	Struthers-Dunn RR1A reed relay
Q1,2,4,5,6,8,10	2N3566 NPN transistor
Q3,7,9	2N3638 PNP transistor
R1,23	100 kΩ , 1/2 W, 1% film resistor
R2	10 kΩ Helitrim 89WR potentiometer
R3	6.8 kΩ resistor
R4,10	150 kΩ resistor
R5,14,22	3.9 kΩ resistor
R6	5.6 kΩ resistor
R7	1 MΩ resistor
R8,9,12	12 kΩ resistor
R11	2.2 kΩ resistor
R13	33 kΩ resistor
R15,19,21	390Ω resistor
R16	50 kΩ Helitrim 89WR potentiometer
R17,20	47 kΩ resistor
R18	1.2 kΩ resistor
R24	2.2 MΩ resistor

Note: All resistors are 1/2 watt, 10% tolerance unless otherwise specified.

MOD 4 SYNCODER

CIRCUIT DESCRIPTION

The design goal for the Mod 4 syncoder was to take advantage of the state-of-the-art improvement in integrated circuit technology and produce a syncoder which had continuously variable time constants for setting the output pulse width and the encoding threshold time constant and in which the synapse output signal, S(t), could be applied to the encoding section in either polarity. In addition, an effort was made to improve the power supply decoupling between boards in the C² syncoder network simulator system. The circuit schematic is shown in Figure 25; the circuit board layout is shown in Figures 26 and 27; and the components are listed in Table 9.

The synapse section of the Mod 4 syncoder is contained in IC1, IC2, and S1. IC1, with its pluggable components R1 and C1, serves as the low pass filter and summing amplifier which generates the synapse output signal, S(t). The output of IC1 is connected to pin C, and thereby to the white holes on the patch panel. Since the summing junction of IC1 is connected to the green holes on the program patch panel through pin B of the circuit board, any components plugged between the white and green holes, appear in parallel with R1 and C1 and can be used to control the low pass filter characteristic of IC1. IC2 serves as a unity gain inverter for S(t). Switch S1 selects whether S(t) from IC1 or $-S(t)$ from IC2 is applied to the input of the encoding section through R4.

Relay K1 can be selected by the PDP-8S computer to apply the encoder input signal (either S(t) or $-S(t)$ depending upon setting of S1) to the C² analog-to-digital converter. Thus, the PDP-8S can sample the output of the synapse section at any time.

The encoding section of the Mod 4 board contains three functional elements. IC3 is the primary element of the comparator stage, IC4 is the primary component of the output one-shot stage, and IC5 is the primary element of the threshold generator stage.

In the Mod 4 encoder, the threshold voltage, T(t), is a negative voltage generated at pin 6 of IC5. This voltage produces a current through R5 which is used to sink the current generated through R4 from S(t). Whenever the current resulting from S(t) exceeds the current resulting from T(t), pin 3 of IC3 tends to go positive. At that time, positive feedback through R6 and C3 causes IC3 to regeneratively latch into a stable state where its output is high. Diodes D1 and D2 at the input of IC3 serve to limit the maximum differential input voltage which may be generated between pins 2 and 3 to less than 1 volt in absolute amplitude and thereby protect the input stage to IC3. For voltages with an absolute amplitude less than about 400 millivolts, diodes D1 and D2 are non-conducting and can be ignored. Thus, at the time when the current from S(t) exceeds the current from T(t), IC3 operates as if those two diodes were not there. It should be pointed out here that both IC3 and IC4 are operational transconductance amplifiers, and that their maximum output current capability is limited by R7 and R13, respectively, to 500 microamperes. When IC3 latches in its high state, it supplies current to R19 in parallel with the series impedance of D3 and R20. Thus, the maximum positive output voltage of IC3 is about $+3.1$ volts. Because of the voltage drop across D3, the voltage applied to IC4 to trigger an output pulse is about $+2.5$ volts. The maximum negative output voltage of IC3 is -5 volts. C4 is used to reduce the high frequency gain of IC3 and prevent RF oscillations.

A comment about the comparator used in this circuit is in order. The generic syncoder concept (discussed in The Syncoder Concept) assumes a voltage comparator which continuously compares S(t) with T(t) and generates an output pulse whenever equality is sensed. In the Mod 4 encoder, the comparator actually compares the currents S(t)/R4 and T(t)/R5. If R4 were equal to R5, then the current comparison would be equivalent to the voltage comparison. However, since R5 is smaller than R4, T(t) is weighted more heavily than S(t) in comparator The effect of this weighting is shown by calculating the equivalent reset voltage for T(t) assuming a voltage comparator and S(t) as a reference voltage. The threshold reset using voltage compared with the IC3 output saturation voltage of $+14$ volts for S(t) determines the minimum duration of the absolute refractory period. With present component values, the -11 volt reset voltage on C6 generates -1.6 milliamperes of comparator current, while the $+14$ volt saturation voltage on IC1 generates 1.4 milliamperes of current. Thus, on an equivalent voltage basis, one could say T(t) resets to -16 volts and S(t) saturates at $+14$ volts. Thus the absolute refactory period equals the output pulse width plus the time it takes for the apparent value of T(t) to decay from -16 to -14 volts. By changing the value of R4 or of R5, the equivalent relationship between maximum saturation voltage of S(t) and reset voltage of T(t) can be easily manipulated. This may be of interest to certain kinds of information processing problems in syncoder networks programmed on C².

IC4 is a current-limited operational transconductance amplifier to which a unity voltage gain current amplifier has been added to simulate an operational amplifier with a high gain-bandwidth product and a slewing rate of nearly 50 volts per microsecond. IC4 supplies the voltage gain, and transistors Q2 and Q3 supply the required current gain. The encoder pulse output through pin J is accessible on the program patch panel through the red holes, and is short-circuit protected by R11 and R12. For purposes of internal feedback, the encoder pulse output is taken directly from the emitter of Q2, and is not short-circuit protected by R11. There are two feedback pathways. The positive feedback is through the resistive voltage divider formed by R14 and R20. The negative feedback pathway is through the RC voltage divider formed by the series resistance of D4, R31, and R10, and the capacitor C5. The operational amplifier circuit so defined is a conventional op amp monostable multivibrator. When a positive trigger is applied to the positive input terminal, the output starts to rise at a rate determined by the gain and slewing rate of the operational amplifier. Since the voltage across C5 can not change instantaneously, at some point during the rising phase, the voltage across R20 exceeds that across C5 and the circuit latches into a metastable state with the

output high and voltage at the positive input higher than the voltage at the negative input. While in this state, the voltage across C5 rises towards the output voltage with a time constant of (R31 + R10)•(C5). Note that during the time when the output is high, Q1 is reverse biased through R9 and can be ignored. When the rising voltage on C5 exceeds the 4-volt reference level maintained across R20, the op amp output voltage starts to fall. Once again, the voltage across C5 can not change instantly, so the falling voltage across R20 causes the circuit to latch in a stable state with the output negative and with C5 discharging toward the negative voltage across R20. Since D4 is reverse biased, C5 can not discharge through R10 and R31. However, when the output goes negative enough, Q1 turns on and C5 is rapidly discharged. In the quiescent state, Q1 saturates and the voltage across C5 is clamped very close to zero. Since the positive feedback through R14 and R20 holds pin 3 of IC4 at − 4 volts, the circuit remains in its low state until the next time that IC3 goes high and triggers an output pulse. Note that by varying R31, the output pulse width can be varied by more than 46 to 1 over the range from 30 microseconds to 1.5 milliseconds.

The threshold circuit is reset with every output pulse. Between output pulses, IC4 is in its low state with Q3 saturated so that diode D6 is reverse biased. There is no input current to IC5. With no input current to its summing junction, IC5 does not supply any feedback current through its feedback impedance. Thus, since pin 2 of IC5 is maintained at virtual ground potential, pin 6 of IC2 is maintained at a voltage equal to the voltage across C6. Any current required by R5 is supplied by the operational amplifier, and the voltage across C6 decays exponentially with a time constant equal to (R15 + R33)•(C6). This time constant can be varied over a continuous range of more than 20 to 1 by varying R33. At the beginning of an output pulse, Q2 saturates, forward biasing D6 and injecting current into the summing junction of IC5 through R16. IC5 supplies an equal and opposite current to the summing junction through D5, C6, and R15 in series with potentiometer R33, thereby producing a negative going waveform while C6 charges toward − (12)•(R33 + R15)/(R16) volts with a time constant of (R33 + R15)•(C6). When this waveform reaches − 11 volts, zener diode D5 starts to conduct and clamps the voltage across C6 at − 11 volts until the end of the output pulse. When the output pulse ends and Q3 saturates again, diode D6 is reverse biased so that no current is injected to the summing junction. Thus, C6 is free to discharge through R33 and R15 until the comparator fires again to restart the whole cycle.

Nothing has been said yet about when the comparator returns to its low or quiescent state during the active timing cycle. In the discussion of output pulse duration, it was implicitly assumed that IC3 returns to its low state before the end of the encoder active state, so that the reference voltage at which IC4 ends the pulse is determined only by R14 and R16. In fact, this is the case; but it is of interest to explain why. First, S(t) is the output of a low pass filter, and as such usually does not contain steep rising voltage waveforms. Thus, during the time between initiation of an output pulse when IC3 senses that S(t) = T(t), and the time that the active state of the output one-shot circuit is reached, S(t) can be assumed to be very nearly constant in value. As soon as the active state is reached, C6 is rapidly charged towards its − 11 volt reset value. Thus, very near the beginning of the active state, the effective value T(t) exceeds the effective value of S(t) and IC3 returns to its quiescent state. However, even if S(t) had a positive step discontinuity at the time of triggering, IC3 would have to return to its quiescent state before the end of the active state due to the way component values were chosen. The maximum time required to fully charge C6 occurs if C6 is initially fully discharged. Under that condition, T(t) may be given by the following expression in which Rf is defined to be equal to (R33 + R15):

$$T(t) = -(12)\,(Rf)\,(1-\exp(-t/(Rf \bullet C6)))/R16$$

Since zener diode D5 clips this waveform when T(t) reaches − 11 volts, the expression above can be approximated to a very high degree of accuracy by:

$$T(t) \simeq \frac{-(12)(Rf)}{R16}\ \frac{(t)}{(Rf)(C6)} = \frac{-(3.6363 \times 10^{-3})t}{(C6)}$$

Setting $T(t)_{max}$ − 11 volts and solving for the time it takes to charge capacitor C6,

$$t_{max} = \frac{(11)(C6)}{(3.6363 \times 10^{-3})} = (3025)(C6)$$

Thus, the worst case charging time with C6 = 0.01 microfarads is 30.25 microseconds. Since the pulse width generated by IC4 is always longer than 30 microseconds, and since the maximum effective value of T(t) is greater than the maximum effective value of S(t), IC3 must always be reset before the end of the output pulse. If C6 is changed to alter the operating range of threshold time constant, care should be used that C5 is also properly chosen. Otherwise the pulse width adjustment set by R31 may interact with the time constant adjustment set by R33.

CHECKOUT PROCEDURE

1. Apply a 2 V 1 kHz sine wave to pin B through a 100 kΩ resistor. Observe a 1 kHz sine wave with inverted polarity but with the same amplitude at pin C to verify operation of IC1.
2. Observe no signal at pin E, unless relay K1 is closed, which verifies the operation of D8, D9, and K1.
3. While observing the sine wave at pin E with relay K1 closed, operate switch S1. If both normal and inverted versions of sine wave can be produced at pin E by switching S1, then IC2 and S1 are working properly.

4. Turn potentiometers R33 and R31 fully clockwise to their maximum value. Vary the amplitude of the input sine wave while monitoring the ± 12V encoder output pulse on a pin J. The output pulse train should be phase locked to the input sine wave in such a manner that interpulse intervals are integer multiples of 1 ms. This verifies operation of the encoder section.

5. Apply + 6 V to pin B through a 100 kΩ resistor, and set switch S1 so that + 6 V appears at pin E with the relay closed. Observe the waveform at pin 6 of IC5 and verify that T(t) starts at − 11 V and decays to − 4 V between output pulses. This verifies operation of IC5, D5, and D6. Note, the time it takes T(t) to decay from − 11 V to − 4 V is equal to one encoding time constant.

6. Connect the ± 12 V pulse output from pin J to an oscilloscope or a digital counter so that pulse width and pulse interval can be measured. The pulse width is the time between a rising edge and a falling edge of the ouput waveform, and should now read 1.4 ms. The time between the falling edge and the rising edge of the output waveform is the encoding threshold time constant and should now read 10 ms.

7. Manipulate switch S1 to inhibit the ouput of the encoder under test. Monitor pin 6 of IC5 while adjusting R32 to zero the output of IC5 (± 5 mV). This verifies operation of R32 and IC5. This adjusts the encoding threshold offset voltage.

8. Reconnect the + 6 V signal to pin B through a 100 kΩ resistor. Observe the zero to + 12 V output waveform on pin H as R31 is turned counterclockwise. The pulse width should decrease smoothly from 1.4 ms to 33 ms, and the encoding threshold time constant should not change from 10 miliseconds. This step verifies operation of R31, Q1, D4, and C5.

9. Observe the output waveform on pin H as J as R33 is turned counterclockwise. The output pulse width should remain constant as the interpulse interval varies smoothly from 10 ms to 470 μs. This verifies operation of D6, D5 and R33.

10. Manipulate switch S1 to inhibit firing of the encoder under test. Measure the DC output voltage of IC5. It should be within ± 5 mV of ground. This verifies operation of IC5.

11. Manipulate switch S1 again to produce output pulses on the syncoder under test. Leave R33 fully counterclockwise and turn R31 clockwise until 50% duty cycle pulse output is achieved watching to be sure that interpulse interval remains equal to 470 microseconds. Short the output at pin J for 10 seconds. Remove the short and observe that the ± 12 V output waveform remains unchanged. This verifies operation of IC4, Q2 and Q3.

12. IC3, IC4 and their associated components are not checked explicitly in this test procedure. If all other tests have been passed, then components are working properly. If there seems to be a problem in this section of the board, start by observing the waveform at pin 3 of IC3. It should never exceed ± 800 mV. If it does, then either D1 or D2 is open, and IC3 may be damaged as a result. Whenever the voltage at pin 3 of IC3 goes through zero with positive slope, a positive pulse should appear at pin 6 of IC3. If not, then IC3 is bad. If the positive pulse appears across R20 but not at the output of IC4, IC4 is bad.

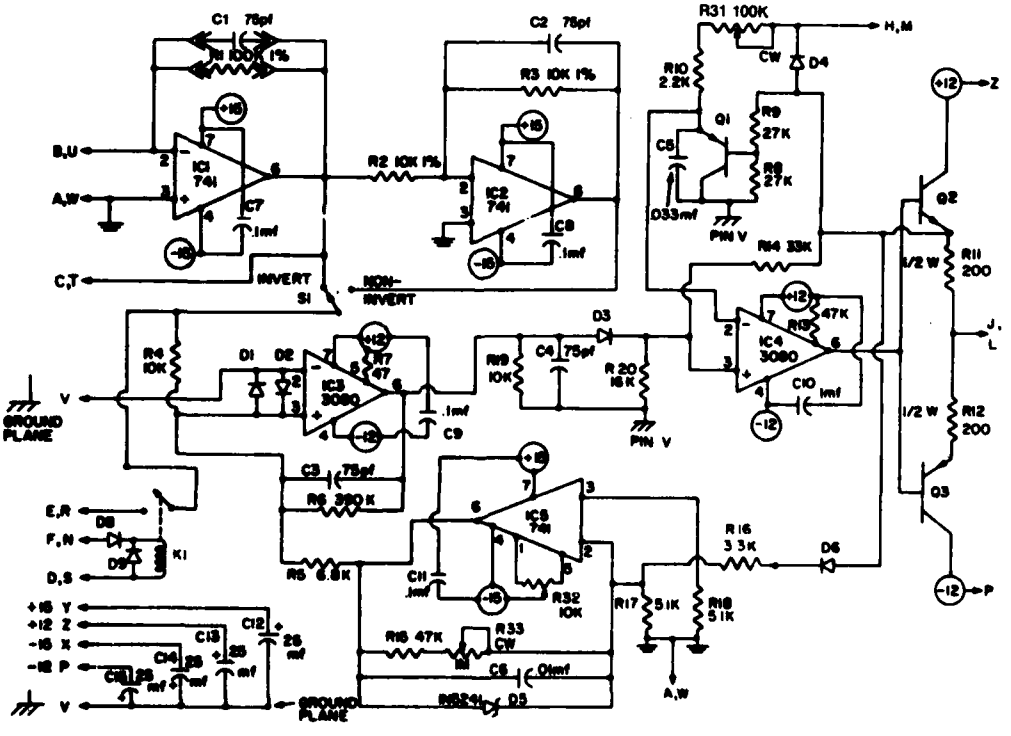


Figure 25. Mod 4 Syncoder Circuit

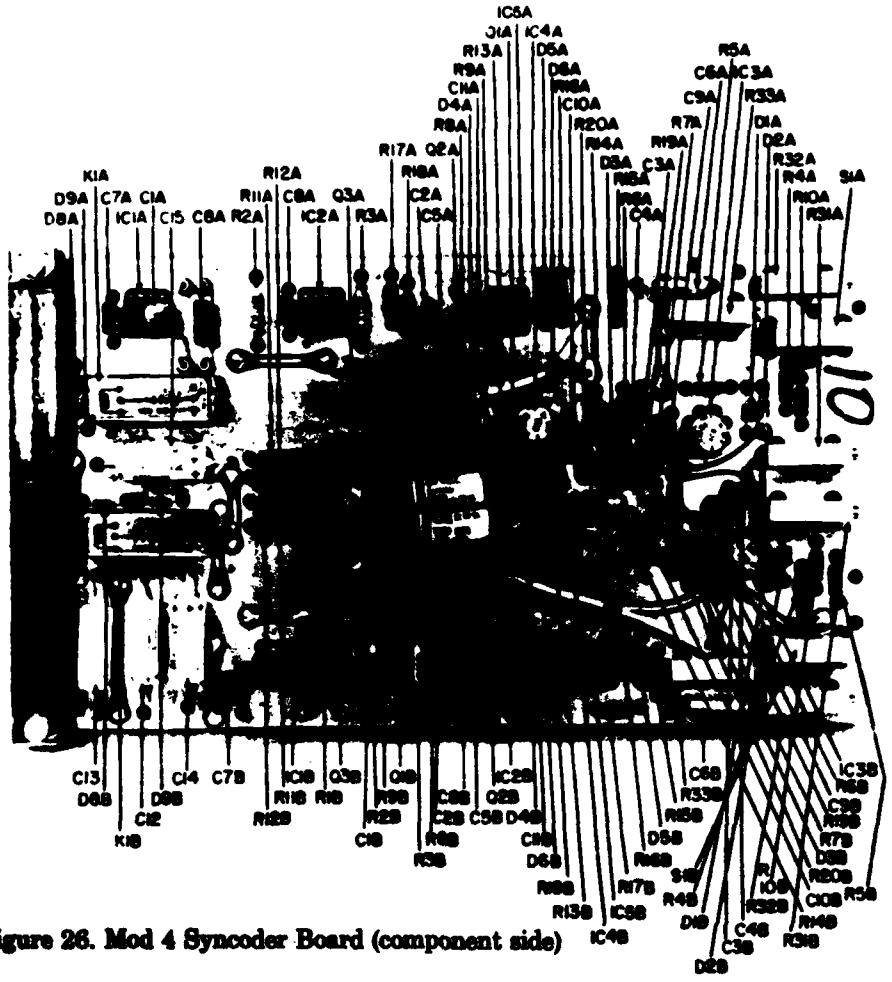


Figure 26. Mod 4 Syncoder Board (component side)

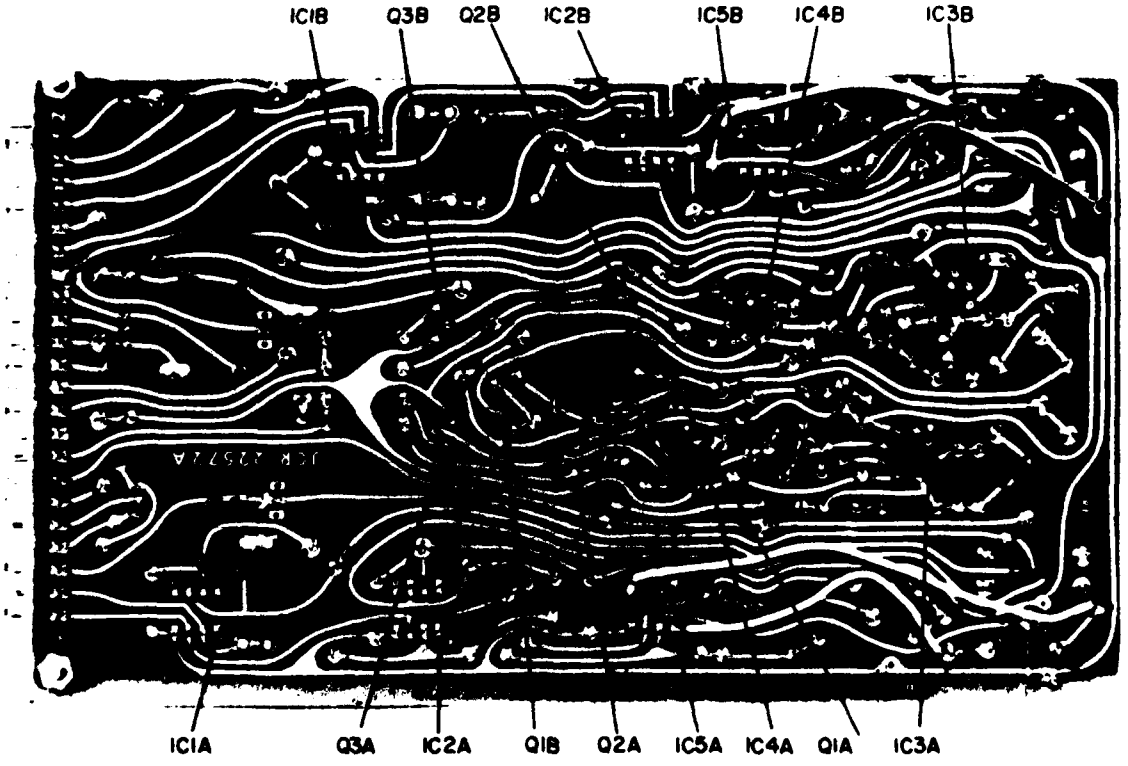


Figure 27. Mod 4 Syncoder Board (foil side)

Table 9. Components for the Mod 4 Syncoder Circuit

Designation	Description
C1,2,3,4	75 pF ceramic capacitor
C5	.033 μF mylar capacitor
C6	.01 μF mylar capacitor
C7,8,9,10,11	.1 μF ceramic capacitor
C12,13,14,15	25 μF, 25 V electrolytic capacitor
D1,2,3,4,6,8,9	1N4154 diode
D5	1N5241 zener diode
IC1,2,5	741 operational amplifier
IC3,4	RCA CA3080 operational amplifier
K1	Struthers-Dunn MRRN1A reed relay
Q1,3	2N3638A PNP transistor
Q2	2N3643 NPN transistor
R1	100 kΩ , 1/8 W, 1% film resistor
R2,3	10 kΩ , 1/8 W, 1% film resistor
R4,19	10 kΩ resistor
R5	6.8 kΩ resistor
R6	390 kΩ resistor
R7,13,15	47 kΩ resistor
R8,9	27 kΩ resistor
R10	2.2 KΩ resistor
R11,12	200Ω , 1/2 W, 5% resistor
R14	33 kΩ resistor
R16	3.3 kΩ resistor
R17,18	5.1 kΩ resistor
R20	16 kΩ resistor
R31	100 kΩ Helitrim 89WR potentiometer
R32	10 kΩ Helitrm 89WR potentiomenter
R33	1 MΩ Helitrim 89WR potentiometer
S1	Alco MSS-1200RG SPDT slide switch

NOTE: All resistors are 1/4 watt, 5% tolerance unless otherwise specified.

MOD 5 SYNCODER

CIRCUIT DESCRIPTION

The goal with the Mod 5 syncoder was to maintain or extend the range of variation of both the output pulse width and the encoding threshold time constant which had been achieved in the Mod 4 circuit, and to simplify the circuit in a manner which might eventually permit fabrication as either a monolithic or a hybrid integrated circuit. The synapse section remains unchanged from the Mod 4 circuit, but the encoding section is completely different. The schematic for the Mod 5 circuit is shown in Figure 28; the board layout is shown in Figures 29 and 30; and the components are listed in Table 10. One capacitor, C11, is used to control both the encoding threshold time constant, and the output pulse width. One operational amplifier, IC3, is used both as the comparator stage and as the output one-shot stage. CMOS analog switches are used to change the character of the feedback around the op amp and thereby control its function either as a comparator or as a one-shot state at the appropriate times.

The CMOS analog switches used in this design are packaged four to a chip, and two switches each from IC4 and IC5 are used in each of the two encoders on each board. Thus, for example switch S1 for encoder A on the left half of the circuit board when looking toward the component side uses pins, 3, 4, and 5 of IC5, while switch S1 for encoder B on the same board uses pins 6, 8, and 9. Other switches are identified in the same manner.

The synapse integrator function is performed by IC1. All analog signals and synapse button signals applied to the summing junction of IC1 are summed in the RC network plugged into the feedback loop around IC1. The resulting waveform S(t) is brought out to the green holes in the C^3 patch panel through syncoder board pin C. S(t) is also used as input to the unity gain inverter comprised of R2, R3, C5, and IC2. Both S(t) and —S(t) are available at switch S1, and either can be selected as input to the encoding section of the Mod 5 syncoder. Relay K1 may be closed by the PDP-8S computer in order to permit the analog-digital converter to measure the voltage applied to the input of the encoder.

The voltage across C11 represents T(t), the threshold voltage, between pulses. T(t) is connected directly to the negative input of IC3 where it is continuously compared with the analog signal S(t) which is applied to the positive input of IC3. As long as T(t) is more positive than S(t), the output of IC3 remains latched at its negative saturation level near − 10 volts. Thus, the encoder pulse output at pin J remains in its quiescent low state between output pulses.

Resistor R9 provides short circuit protection for the output. T(t) decays exponentially towards zero volts as the charge stored on C11 leaks off through S1 and R6. When S(t) exceeds T(t) by a small amount, the output of IC3 starts to go positive. This initiates a chain of events which lead to a change in configuration for IC3. The positive edge of the output pulse is differentiated by C12, R11, and R12. The resulting positive spike is used to momentarily close the normally open switches S2 and S3 on IC4. S2 causes C11 to rapidly discharge, producing a positive feedback signal to the comparator which insures regenerative turn-on once the initial turn-on condition is sensed. A more direct positive feedback signal is applied as soon as the rising pulse output waveform exceeds the value of S(t) so that diode D2 is turned on. D2 clamps the positive input of IC3 to a level, one diode voltage drop below the positive saturation voltage of IC3, effectively disconnecting S(t) from the op amp. Since C11 is discharging through S2 at that point, the operational amplifier circuit latches into a stable state with its output high. During the time that C11 is discharging through S2, switch S3 remains closed and prevents the positive pulse output signal from closing switch S4. As the positive spike across R12 decays, switches S2 and S3 open. As S3 opens, the positive drive signal from the pulse output is applied to the control gates of S1 and S4 through R10 causing S1 to open and S4 to close. With S1, S2, and S3 all open, and S4 closed, C11 charges exponentially towards + 12 volts with a time constant of (R5 + R8)•(C11). IC3 continuously compares this rising exponential waveform, which is applied to its negative input, with the positive reference voltage clamped to its positive input by diode D2. When the voltage across C11 exceeds the reference voltage level, the output changes state and returns to its negative saturation level. The negative pulse output voltage applied through R10 returns switches S1 and S4 to their quiescent conditions, and causes diode D2 to be reverse biased into cutoff so that S(t) is once more applied to the positive input of IC3 through R4. With S1 closed the voltage across C11 again decays towards zero with a time constant of (R6 + R7)•(C11) until such time as S(t) exceeds T(t) to reinitiate the cycle.

A word of caution concerning the CMOS switches is in order. These devices are rated to operate with input and output signals limited the applied power supply voltages. In this circuit the power supply for CMOS is taken between 0 and + 12 volts. Switches S1, S2, and S4 are all operated with signal and control voltage levels limited within the proper range. Under transient conditions negative drive signals may be generated by capacitive coupling of pulse edges at various points in the circuit. In every case where this is possible, there are series resistances of at least 10,000 ohms to limit the resulting current to a value which can be safely handled by the gate protection diodes built into the CMOS circuits. The resistors also limit the transient current to the value less than the peak point current required to activate the internal parasitic diodes. If triggered, these diodes can latch up in a condition where the power supply is internally short circuited resulting in self destruction of the chip. Any attempt to change the resistor values in this circuit could prove disastrous unless these CMOS switches are first replaced by the far-more expensive version manufactured with silicon-on-sapphire floating body technology. Between pulses, the − 12 volts applied to R10 may appear to pose a threat to switch S3. However, the gate protection diodes on switches S1 and S4 prevent the signal at pins 3 and 10 of IC4 from becoming negative enough to cause any damage.

The ± 12 volt syncoder pulse output in this circuit is taken directly from the output of IC3 through resistor R9. The zero to + 12 volt pulse output used for driving the neon drivers in C^2 is extracted from this signal across diode D3.

CHECKOUT PROCEDURE

1. Apply a 2 V 1 kHz sine wave to pin B through a 100 kΩ resistor. Observe the sine wave inverted but otherwise unchanged at pin C to verify the operation of IC1.
2. Synchronizing off of the oscillator, monitor pin E. There should be no signal until relay K1 is closed. With K1 closed, manipulate switch S1 and observe both normal and inverted polarity of the sine wave at pin E. This verifies operation of K1, S1 and IC2.
3. Turn potentiometers R6 and R8 fully clockwise to their maximum resistances. Observe ± 12 V pulses at pin H to verify operation of the encoder section, and 0 to + 12 volt pulses at pin H to verify operation of D3.
4. Monitor the interpulse interval of the output pulse train as the amplitude of the sine wave is varied. The output pulse interval should phase lock to the 1 kHz input signal with intervals which are integer multiples of 1 ms. This is further verification of proper encoder operation.
5. Using a 10 MΩ oscilloscope probe, monitor the voltage across C11 (pin 2 of IC3). At the beginning of each pulse, C11 should be fully discharged to ground. Then C11 should charge exponentially towards the + 12 V power supply level through R5 and R8. At about + 11 V, the charging cycle should stop, and C11 should discharge towards ground through R6 and R7. This verifies operation of all CMOS circuits. Measure the maximum charging voltage and record its value. Remove the oscilloscope probe.
6. Apply + 4 V to pin B through a 100 kΩ resistor, and set switch S1 so that + 4 V is applied to the encoder input (pin E with relay K1 closed). Be sure the other encoder is inhibited and not firing. Monitor the output pulse train at pin J with an oscilloscope or electronic counter and measure the pulsewidth and interpulse interval, which should be equal to the encoding threshold time constant. For C11 = 0.0033 μF, the pulsewidth should be around

780 μs and the time constant about 2.3 ms. For C11 = 0.01 μF, the pulsewidth should be 2.5 μs and the time constant, 1 μs.

7. Manipulate switch S1 to inhibit the encoder under test. Measure the voltage across C11 to verify that it is equal to zero (± 5 mV). If it is not, then one of the CMOS switches is malfunctioning and needs to be replaced.

8. Now manipulate switch S1 to excite the encoder under test. Slowly turn R8 counterclockwise shortening the output pulsewidth while watching to be sure that the interpulse interval remains constant. With R8 fully counterclockwise, the pulsewidth should be 42 μs for C11 = 0.0033 and 75 μs for C11 = 0.01. This verifies the operation of R8.

9. Now turn R6 slowly counterclockwise shortening the interpulse interval while watching to be sure the output pulsewidth remains constant. With R6 fully counterclockwise, the interpulse interval should be 33 μs for C11 = 0.0033 and 79 μs for C11 = 0.01. This verifies the operation of R6.

10. Reconnect the 10 MΩ scope probe to C11 and monitor the voltage across C11 as the DC input voltage is varied between zero and + 10 V. C11 should fully discharge at the beginning of the pulse for all levels of input voltage and recharge to the same voltage level near + 11 V for all values of input voltage.

This completes the Mod 5 checkout.

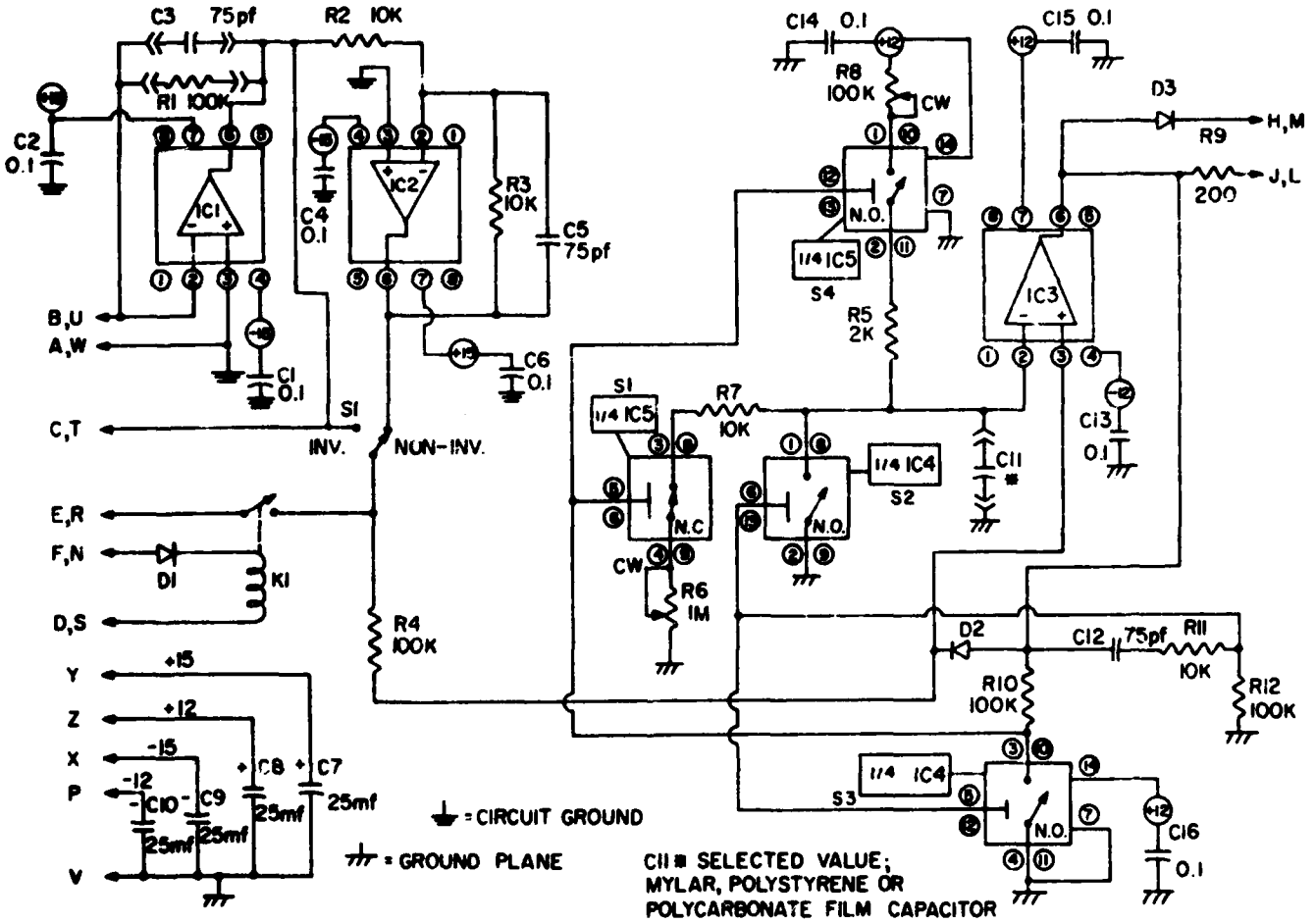


Figure 28. Mod 5 Syncoder Circuit

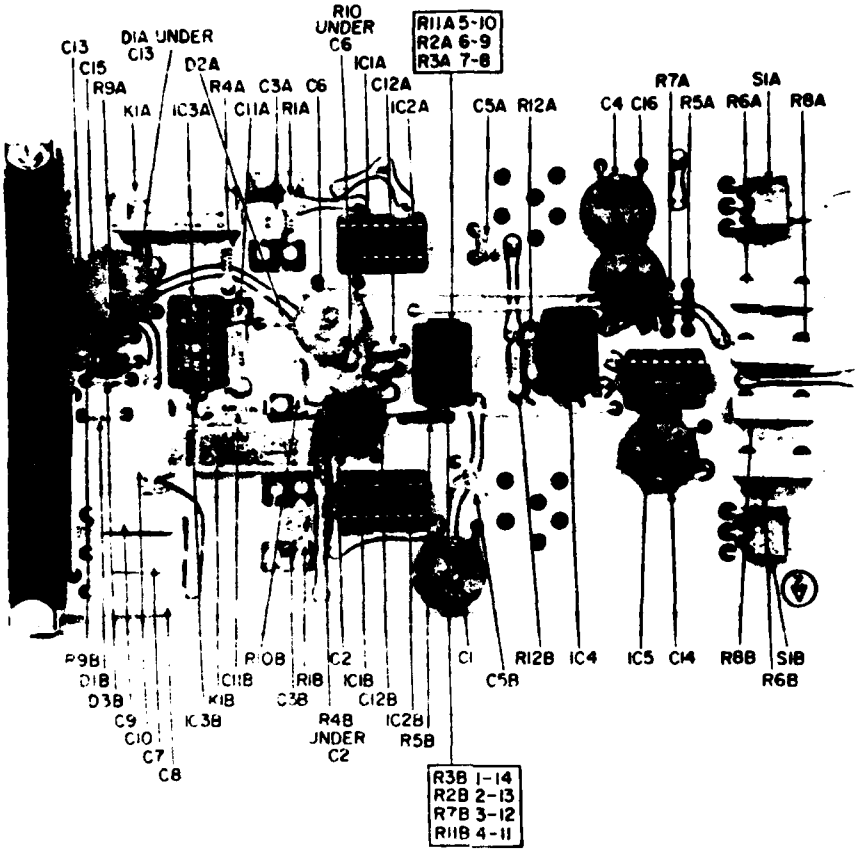


Figure 29. Mod 5 Syncoder Board (component side)

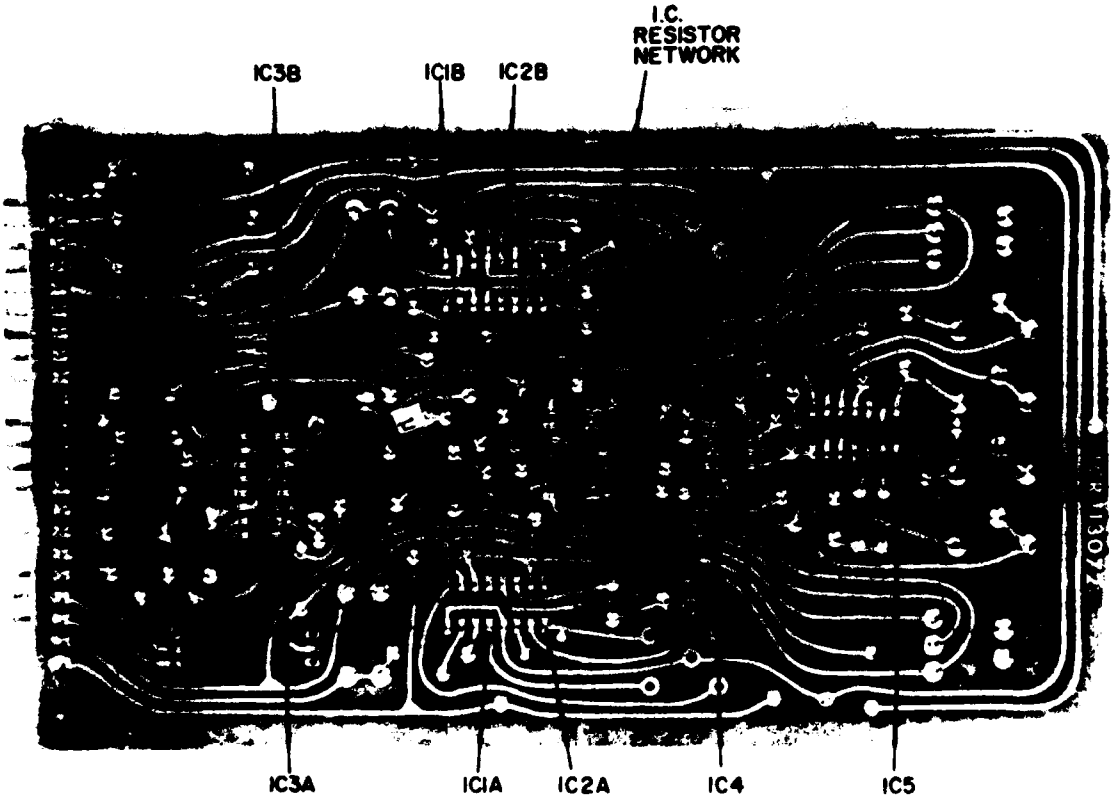


Figure 30. Mod 5 Syncoder Board (foil side)

Table 10. Components for the Mod 5 Syncoder Circuit

Designation	Description
C1,2,4,6,13,14, 15,16	.1 μ F ceramic capacitor
C3*5,12	75 pF ceramic capacitor
C7,8,9,10	Mallory MTA25D20 25 μF, 20 VDC capacitor
C11*	.0033 μF mylar capacitor
D1,2,3	1N4154 diode
IC1,2	LM741CN operational amplifier
IC3	LM301AN operational amplifier
IC4	CD4016AE CMOS switch
IC5	SCL4416AE CMOS switch
K1	Struthers-Dunn MRRN1A reed relay
R1,4,10,12	100 kΩ , 1/4 W, 1% resistor
R2,3,7B,11	Allen Bradley 10 kΩ resistor network
R5	2 kΩ , 1/4 W, 5% resistor
R6	1 MΩ Helitrim 89WR potentiometer
R7A	10 kΩ , 1/4 W, 5% resistor
R8	100 kΩ Helitrim 89WR potentiometer
R9	200Ω , 1/2 W, 5% resistor
S1	C&K 7101A SPDT toggle switch

* R1, C3 and C11 are mounted on terminals and there values may be changed depending on the application of the syncoder.

COMPARISON BETWEEN SYNCODER CIRCUITS

Although all five versions of the syncoder exhibit the same nominal transfer function, there are differences in operation particularly near the extreme limits of the various parameters. Table 11 contains a summary of circuit idiosyncrasies from the point of view of the C^3 programmer. It is intended as an aid in selecting the particular version to be used for various portions of each network.

Table 11. Comparison of Syncoder Circuits

Parameter	Mod 1	Mod 2	Mod 3	Mod 4	Mod 5
1. Synapse Integrator					
a. offset voltage	adjust with R2	adjust with R2	adjust with R2	fixed < 5mV	fixed < 5mV
b. output polarity	inverted	inverted	inverted	selectable	selectable
c. maximum output current, mA	1	5	5	5	5
d. rated load, kΩ	10	2	2	2	2
e. output saturation voltage, V	± 13	± 13	± 14	± 14	± 14
2. Encoder					
a. encoding time constant	10 ms fixed	10 ms fixed	controlled by C5	range set by C6 value by R33	range set set by C11 value by R6
b. output pulse width	1 ms fixed	1 ms fixed	controlled by C4	range set by C5 value by R31	range set by C11 value by R8
c. maximum threshold voltage, V	− 11	− 11	− 11	− 17	+ 11
d. is latch-up possible?	yes	yes	yes	not for R5 less than 7.9kΩ	yes
e. rated load, Ω	390	390	390	200	200
f. maximum output current, mA	15	15	15	30	20
g. maximum fan-out (synapses)	15	15	15	30	30
h. threshold offset voltage	adjust with R16	adjust with R16	adjust with R7	adjust with R32	fixed < 5mV

MOD 1

The Mod 1 circuit is characterized by a fixed output pulse width of 1 millisecond and a fixed encoding threshold time constant of 10 milliseconds, the synapse integrator can supply only 1 milliampere of output current, and so is limited to driving loads of greater than 10,000 ohms. The pulse output can supply 15 milliampere with a 6-volt drop, and so can drive a maximum of 15 C^3 synapse buttons. The initial value of threshold voltage is − 11 volts, and the maximum value of the output of the op amp is 13 volts. With large input signals, it is possible to achieve a latched condition where the pulse output remains high all the time.

MOD 2

The Mod 2 circuit is identical with the Mod 1 except that the synapse integrator is capable of supplying 5 milliamperes of output current, and can therefore drive any load greater than 2,000 ohms.

MOD 3

The Mod 3 circuit has several components mounted in pluggable jacks. The feedback impedence on the synapse integrator may be programmed by plugging different values of resistors, capacitors, or even inductors into the jacks on the board. The encoding threshold time constant is equal to (C5)•(R11 + R13), and can be controlled by plugging in various values of C5. The output pulse width is controlled by C4 and R5. As long as (C4)•(R5) is smaller

than (C5)•(R11), C4 may be chosen at any value to select the output pulse width. If (C4)•(R5) is greater than (C5)•(R11), then the output pulse would end before C5 has a chance to fully charge, and the threshold voltage would be too small immediately after the end of a pulse. the synapse integrator output can supply up to 5 milliamperes and drive any impedance greater than 2,000 ohms. The pulse output can drive up to 15 C³ synapse button loads.

MOD 4

With the Mod 4 syncoder, not only is there the provision for plugging in arbitrary feedback impedances on the circuit board itself; but there is also a switch, S1, which permits the programmer to select the polarity of the encoder input signal by either using or not using the unity gain inverter, IC2. As with all C³ boards, the computer is able to sample the encoder input signal through relay K1. However, with the Mod 4 and Mod 5 boards, the encoder input signal may or may not have the same polarity as the synapse integrator output. The output pulse width is controlled by the time constant (C5)•(R10 + R31), and the encoding threshold time constant is determined by (C6)•(R15 + R33). The output pulse width is continuously variable from 50 microseconds to 1.5 milliseconds with R31. The encoding threshold time constant is continuously variable from 470 microseconds to 10 milliseconds with R33. If the range of operation needs to be changed, it can be changed by soldering in different values of C5 and C6. In order to insure complete recharging of C6 during an output pulse, it is necessary that (C5)(R10) be greater than (C6)•(R16). The analog output can supply 5 milliamperes to loads greater than 2,000 ohms. The pulse output can drive up to 30 C³ synapse buttons. The initial effective value of the threshold in the Mod 4 board is 17 volts, and the maximum output voltage of the synapse integrator is 14 volts. Thus, latch-up is not possible in the Mod 4 board. The effective value of the threshold initial voltage is controlled by changing R5, as explained under Mod 4 circuit description.

MOD 5

The Mod 5 circuit is similar to the Mod 4 in that encoder polarity is switch selectable, both the encoding threshold time constant and the output pulse width are continuously variable with potentiometers, and arbitrary feedback impedances for IC1 may be plugged into the circuit board. The encoder input is available to the PDP-8S computer through relay K1. The threshold initial value is about 11 volts, and the synapse integrator saturation voltage is about 14 volts, so a latch-up condition with large input signals is possible. Both the output pulse width and the encoding threshold time constant are determined by the same capacitor, so the relative value of the ranges of operation are fixed. The Mod 5 boards were constructed in two versions, one with C11 = 0.01 microfarad, and the other with C11 = 0.0033 microfarad. Table 12 shows the range of pulse width and time constant for the Mod 5 Board with these two values of C11. Ranges for other values of C11 may be derived from this Table.

Table 12. Mod 5 Syncoder Pulse Parameters

		C11 = .01 μF	C11 = .0033 μF
Pulsewidth	minimum	75 μs	42 μs
	maximum	2.5 ms	784 μs
Time Constant	minimum	79 μs	33 μs
	maximum	1.01 ms	2.28 ms

The analog output of the synapse integrator can supply up to 5 milliamperes to loads greater than 2,000 ohms. The pulse output can supply up to 30 C³ synapse button switches.

THE C³ SAMPLE-AND-HOLD CIRCUITS

There are four circuits, identified numerically, on each sample-and-hold board. The output pins to the holes on the patch panel are pins W, V, B, and A for circuits 1, 2, 3, and 4, respectively. These boards fill almost all the remaining slots in the card file racks shown in Figure 13. On the left side, row M contains the 17 boards for sample-and-hold locations A1A through A3V, row N for location A3W through B2R, P for B2S through C1M, and R for C1N through C4H. Slots 15 and 16 in row A contain the 2 boards for C4J through C4R with locations C4S through C4Z corresponding to the circuits on boards 15 and 16 in row B. In the right-hand rack, row H contains the boards for sample-and-hold locations D1A through D3V, row J for locations D3W through E2R, K for E2S through F1M, and L for F1N through F4H. Slots 15 and 16 in row E contain the boards for locations F4J through F4R with the remaining locations F4S through F4Z circuits on the boards in slots 15 and 16 of row F.

There are currently two versions of sample-and-hold circuitry. The Mod 1 circuit makes use of a junction field effect transistor source follower with a complementary bipolar transistor voltage amplifier in a feedback loop to achieve a stable unity-gain, high input impedance voltage follower. The Mod 2 circuit uses a commercial FET-input op amp for the same function. The voltage follower acts as an impedance converter between the storage capacitor and the output terminal of the sample-and-hold.

All sample-and-hold relays in C^3 system are connected to a common bus which is driven by the output of the D-A converter. When a relay is closed by the PDP-8S computer, the 1 microfarad storage capacitor charges towards the D-A voltage through a 1,000 ohm resistor with a time constant of 1 millisecond. When the relay is opened by the computer, the capacitor stores this voltage, and the voltage follower supplies current to its load at the stored voltage level.

MOD 1 SAMPLE-AND-HOLD

To understand the operation of the Mod 1 circuit, consider the circuit in Figure 31, where the gate of Q1 is connected to the anode of D102, and the terminal characteristics of the resulting two terminal device are shown. As the voltage across this combination is increased, the current through it also increases until the pinch-off voltage, V_p, is reached. For voltages above the pinch-off voltage, further increases in voltage cause only small increases in the current. This configuration may thus be used as a constant current diode. If the gate of Q1 is disconnected from the anode of D102 and the device is placed in a system in such a manner that the drain current equals the pinch-off current previously mentioned, while the voltage across Q1 is equal to the pinch-off voltage, then the voltage at the anode of D102 will be equal to the voltage at the gate of Q1. This is the principle of the sample-and-hold circuits. The circuit diagram for the Mod 1 version is shown in Figure 32; the circuit board layout is shown in Figures 33 and 34; and the components are listed in Table 13. In operation, the capacitor voltage applied to the gate of Q1 is reproduced at the anode of D102. Q2 and Q4 serve to supply the exact value of current, I_{op}, required by Q1; and Q3 maintains the exact value of voltage, V_{op}, required across Q1 to insure zero offset voltage between the gate of Q1 and the anode of D102.

The voltage across Q1 and D102 is maintained constant by D104 and Q3. D104 serves as a voltage reference, and Q3 serves as an emitter follower to keep the voltage across Q1 and D102 constant and independent of the drain current through Q1. The current through D102 and Q1 is controlled by R104 and RS1, which shall be referred to as RS for the remainder of this discussion. Because of the nature of the feedback loop around RS through Q4 and Q2, there is only one stable value of voltage which can be maintained across RS. If Q2 tries to supply more current than necessary, the voltage across RS increases causing the collector current of Q4 to increase, causing a reduction in the available base current for Q2, and therefore causing the emitter current of Q2 to decrease back to the quiescent value. On the other hand, if Q2 tries to supply less current than necessary, the voltage across RS decreases, causing a decrease in collector current drawn by Q4, causing an increase in base current available to Q2, causing the emitter current of Q2 to increase back to its quiescent value. Thus, the voltage across RS is held at a constant value determined by the forward voltage drop across D103 and the base emitter junction of Q4. By selecting the value of RS, it is possible to select the current which flows through Q1. Thus, at the time of manufacture or repair, pin D is grounded, relay K101 is closed, and RS is adjusted so that the output at pin A is equal to zero volts. In this manner RS is selected to provide the pinch-off current required by Q1 in order that the circuit may acts as a unity gain voltage follower with no voltage offset between input and output.

Since the open loop gain of the amplifier formed by Q4 and Q2 is very high, this circuit is subject to high frequency oscillations if it is not properly compensated. It is the function of C104 to reduce the loop gain of the amplifier below unity gain at the loop natural resonant frequencies and therefore to stabilize the amplifier.

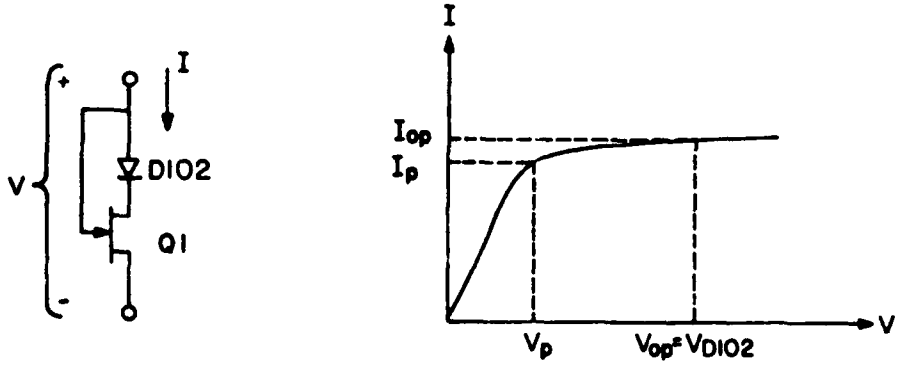


Figure 31. Constant Current Configuration

The current through Q1, I_{op}, is determined by the value of RS and the forward voltage drop through the base of Q4 and diode D103. Since this voltage is highly temperature sensitive, it follows that the operating current is also temperature sensitive. If the voltage across Q1 is maintained constant while the current through Q1 is varied, then the gate voltage of Q1 will not track the anode voltage of D102. However, if the voltage across Q1 is varied as the current through Q1 varies so that I_{op} and V_{op} remain on the curve of Figure 34, then it is possible for the offset voltage between the gate of Q1 and the anode of D1 to remain equal to zero. First order temperature compensation of this circuit is achieved by using the temperature dependence of the forward voltage drop across D102 and the base emitter of Q3 to shift the bias voltage between the drain and the source of Q1 in such a way that the temperature dependence of the bias current established by Q4 and D103 is properly compensated. Because the various PN junctions are not thermally connected and are not carefully matched, the compensation is not perfect and offset voltage does drift with temperature.

The circuit operation depends on the fact that diode D4 operates as a stable voltage reference. In fact, as the input voltage changes, the amount of current available for biasing D104 varies. For a − 10 volt input signal in some units, the current through D104 falls below the zener knee, and the voltage across D104 then drops precipitously. Therefore, not all of the Mod 1 circuits are capable of holding large negative voltages.

In summary, the drift and offset voltages associated with this sample-and-hold circuit are due to several factors. The gate leakage current is the primary component of short term drift, causing about 30 millivolts per minute drift. The offset voltage is affected by the value of the input voltage, since the voltage across D104 is a monotonic function of input voltage. The offset voltage is also a strong function of temperature, since the current through Q1 is determined by the temperature dependent junction voltages of Q4 and D103.

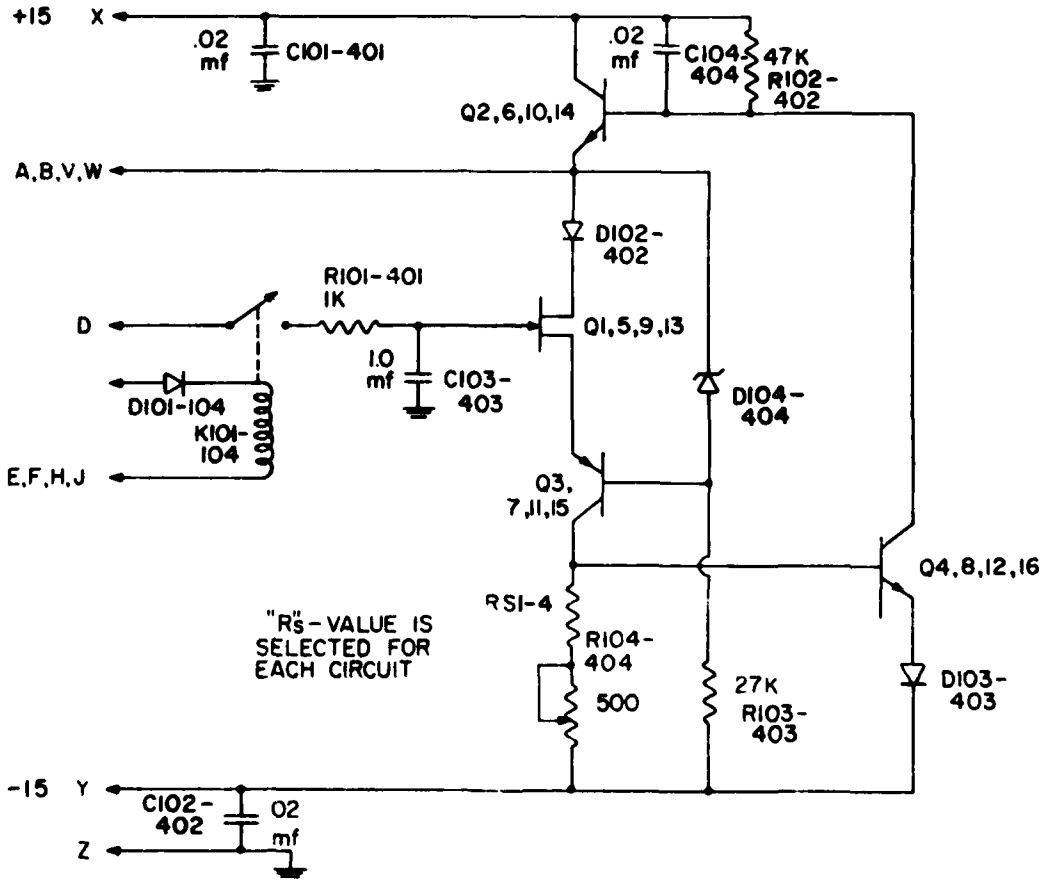


Figure 32. Mod 1 Sample-and-Hold Circuit

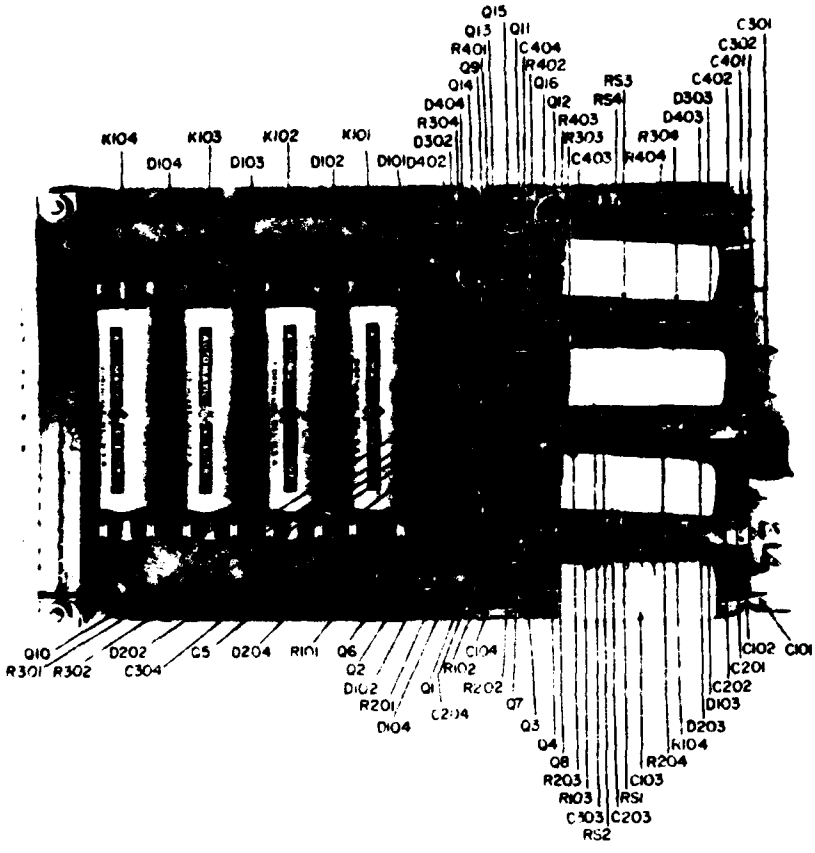


Figure 33. Mod 1 Sample-and-Hold Board (component side)

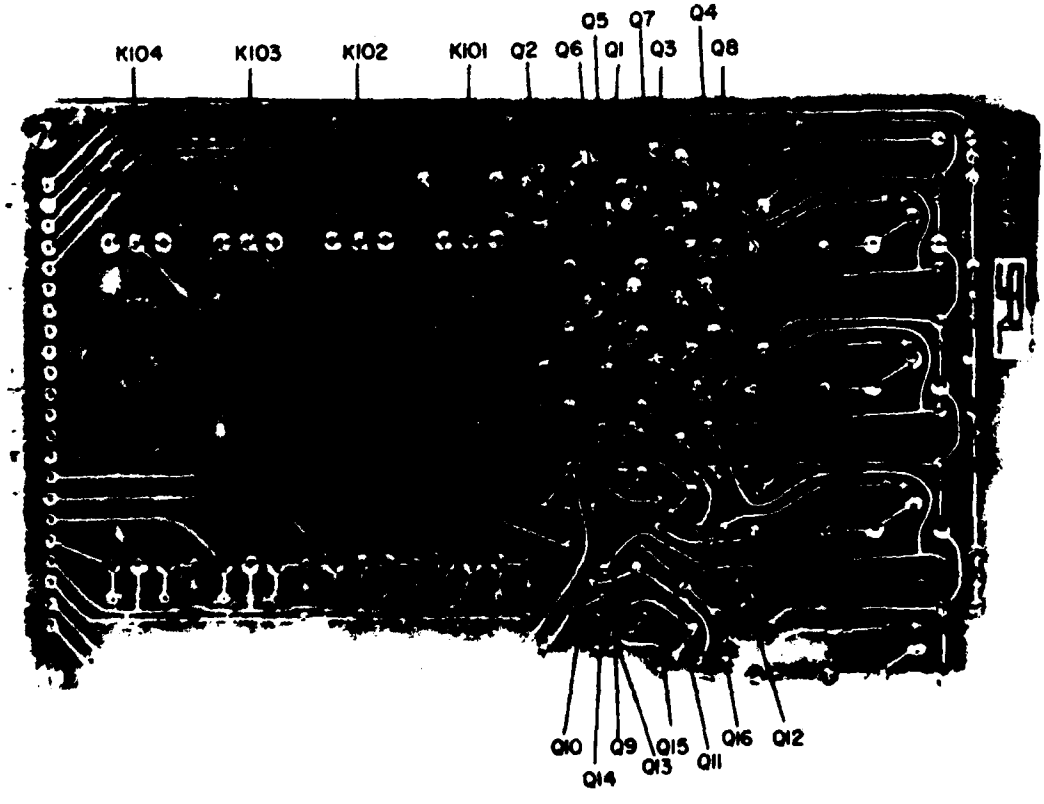


Figure 34. Mod 1 Sample-and-Hold Board (foil side)

Table 13. Components for the Mod 1 Sample-and-Hold Circuit

Designation	Description
C101,102,104	.02 μF ceramic capacitor
C103	1 μF mylar capacitor
D101,102,103	1N4154 diode
D104	1N751 zener diode
K101	Automatic Electric PD13001-9 reed relay
Q1	Fairchild FS20978 field effect transistor
Q2,4	2N3566 NPN transistor
Q3	2N3638 PNP transistor
R101	1 kΩ , 1/2 W, 10% resistor
R102	47 kΩ , 1/2 W, 10% resistor
R103	27 kΩ , 1/2 W, 10% resistor
R104	500Ω Bourns 3067P-1-501 E-Z Trim potentiometer
RS1	1/2 W, 5% resistor, value selected for each circuit

MOD 2 SAMPLE-AND-HOLD

The Mod 2 sample-and-hold circuits (shown schematically in Figure 35 and pictured in Figures 36 and 37 with components listed in Table 14) are plug compatible with the Mod 1 sample-and-hold boards. The circuit makes use of a high quality integrated circuit operational amplifier with a field effect transistor input stage optimized to minimize input bias current, a reed relay, and a low-leakage mylar film capacitor. In the circuit description, all references will be made to components associated with one of the four identical circuits, section 4, shown on the left side of the schematic. All other circuits operate in exactly the same way.

All sample-and-hold board relays are connected to a common signal bus which carries the output of the C^2 digital to analog converter. When the PDP-8S closes the relay to any given sample-and-hold circuit, capacitor C12 charges towards whatever voltage level is currently being supplied from the D-A converter on pin D of the board edge connector. The time constant of the charging cycle is (R12)•(C12) = 1 millisecond. By varying the frequency of the real-time clock, the dwell time may be chosen at any value between 5 and 50 milliseconds. Subtracting the 2 milliseconds required for the relay to close and open, the nominal charging time for C12 varies between 3 and 48 milliseconds. Stated another way, the exponential charging curve runs for an elapsed time of 3 to 48 time constants.

IC4 is connected in the form of a unity gain voltage follower. R11 provides short circuit current protection for the input stage during transient conditions when the differential input voltage may exceed 1/2 volt. During normal operation, R10 can be neglected compared with the 10^{12} ohm input impedance of IC4. Thus, the output voltage of IC4 is equal to the stored voltage of C12. The voltage on C12 decays due to internal leakage in the capacitor, leakage through the operational amplifier, leakage across the printed circuit board, and leakage across the reed relay. The measured voltage drift of this circuit averages about 1 millivolt per minute.

There are two kinds of observable voltage drift in this circuit. If C12 has been fully discharged for some time, and is suddenly charged to + 10 volts, then 10 millivolts of drift during the first minute is usually observed. This is due to dielectric soakage and form factor readjustment going on within the mylar capacitor. These phenomena die out by the end of two minutes and then the drift returns to the 1 millivolt per minute quoted above. The slow drift rate is caused by internal capacitor leakage and op amp bias current, plus the inherent voltage offset drift of the operational amplifier. R10 may be adjusted to minimize the operational amplifier offset voltage for any operating temperature. However, as temperature varies, the amplifier offset varies too.

C10 and C11 are power supply bypass capacitors which serve to protect the amplifier from transients on the power supply bus. They also serve to short circuit high frequency energy which, if not shorted out, can cause oscillations in a system with distributed amplification.

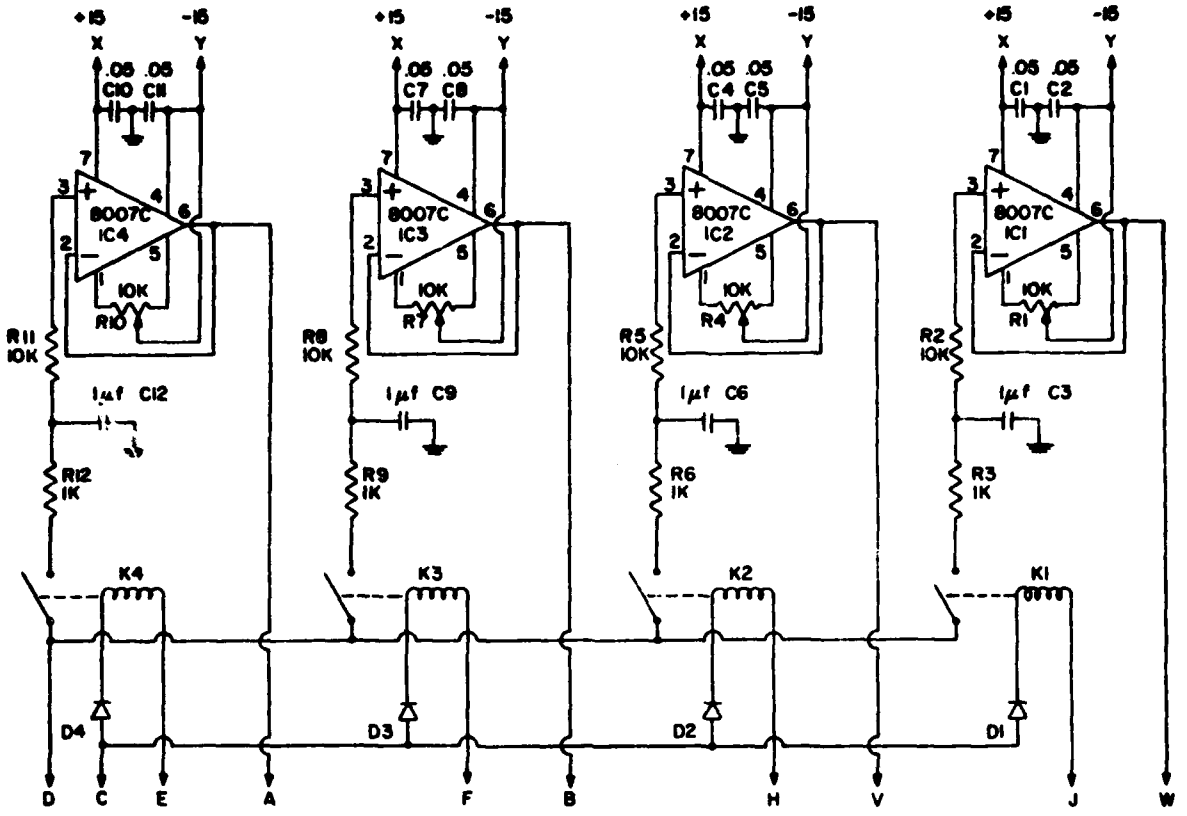


Figure 35. Mod 2 Sample-and-Hold Circuit

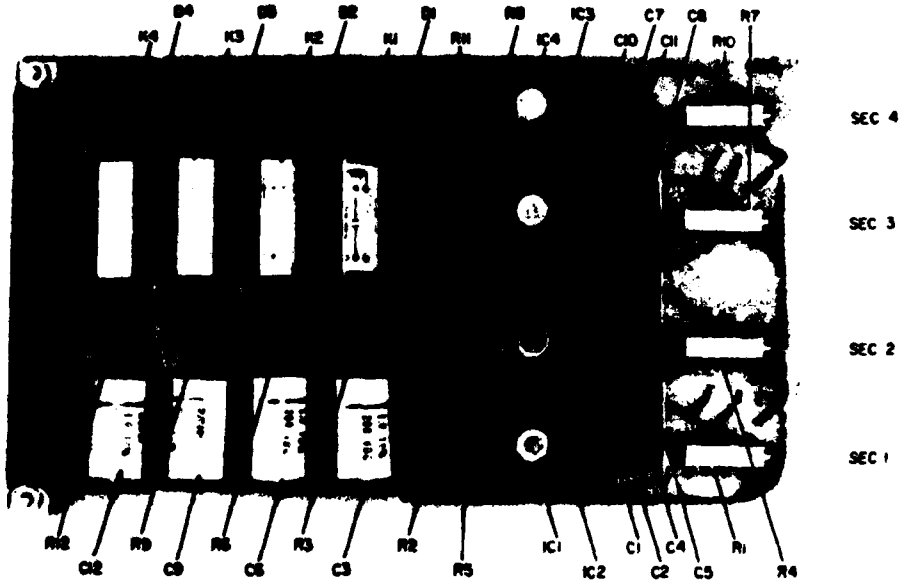


Figure 36. Mod 2 Sample-and-Hold Board (component side)

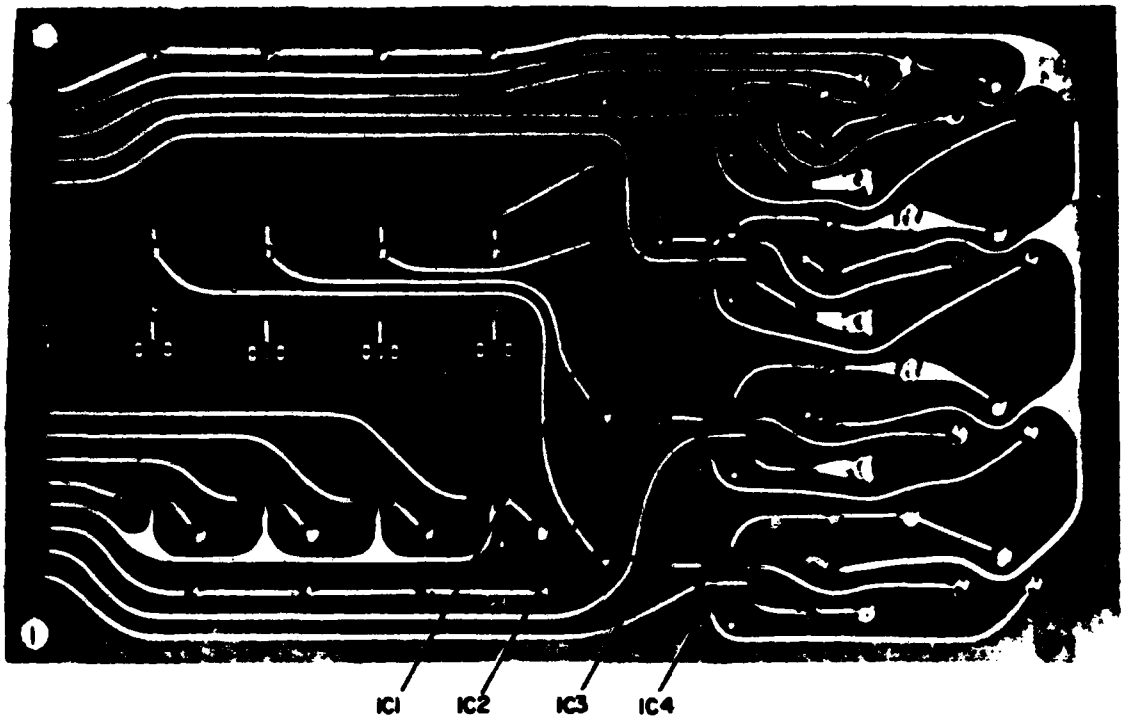


Figure 37. Mod 2 Sample-and-Hold Board (foil side)

Table 14. Components for the Mod 2 Sample-and-Hold Circuit

Designation	Description
C1,2,4,5,7,8,10,11	.05 μF ceramic capacitor
C3,6,9,12	1 μF mylar capacitor
D1,2,3,4	1N4154 diode
IC1,2,3,4	Intersil 8007C operational amplifier
K1,2,3,4	Struthers-Dunn MRRN1A reed relay
R1,4,7,10	10 kΩ Helitrim 89WR potentiometer
R2,5,8,11	10 kΩ 1/4 W, 5% resistor
R3,6,9,12	1 kΩ , 1/4 W, 5% resistor

MISCELLANEOUS C³ CIRCUITS

There are many circuits used in C³ control bay which are not discussed in this report. These circuits are documented in the *Maintenance Manual for "Middle C³" Control System* and, for the most part, are commercially available modules. There are, however, four other circuit board types in the C³ System which have not yet been discussed. They are the extra operational amplifiers, the neon lamp drivers, the power supply isolation capacitors, and the synapse buttons.

EXTRA OPERATIONAL AMPLIFIERS

The synapse integrator section of a syncoder can be used for general analog signal processing, but this ties up the entire syncoder. Also, the Mod 1 syncoder synapse integrator uses a Nexus SQ-10 op amp with a maximum output current of one milliampere. This relatively low value limits the number of syncoders which can be driven with this

analog output. For these reasons, extra op amps were designed into the C³ System. However, all other versions of syncoders have synapse integrator op amps with a 5 milliampere output current capability, so the extra op amps are not required so much for power boosting purposes as for general signal processing.

There are three operational amplifier circuits on each board, identified numerically. (Looking at the component side of the board with the connector at the bottom, circuit #3 is on the left side.) The schematic diagram is shown in Figure 38; the circuit board layout is shown in Figures 39 and 40; and the components are listed in Table 15. Thus, the six extra op amps in each bay, one at the bottom of each section of the patch panels, are contained on two cards, one for each half of the patch panel bay. Referring to Figure 13, the extra op amps for sections A, B, and C are located on the circuit board in slot 16 of row C (circuits 1, 2, and 3, respectively). Correspondingly, the op amps on the board in slot 16 of row D are for sections D, E, and F.

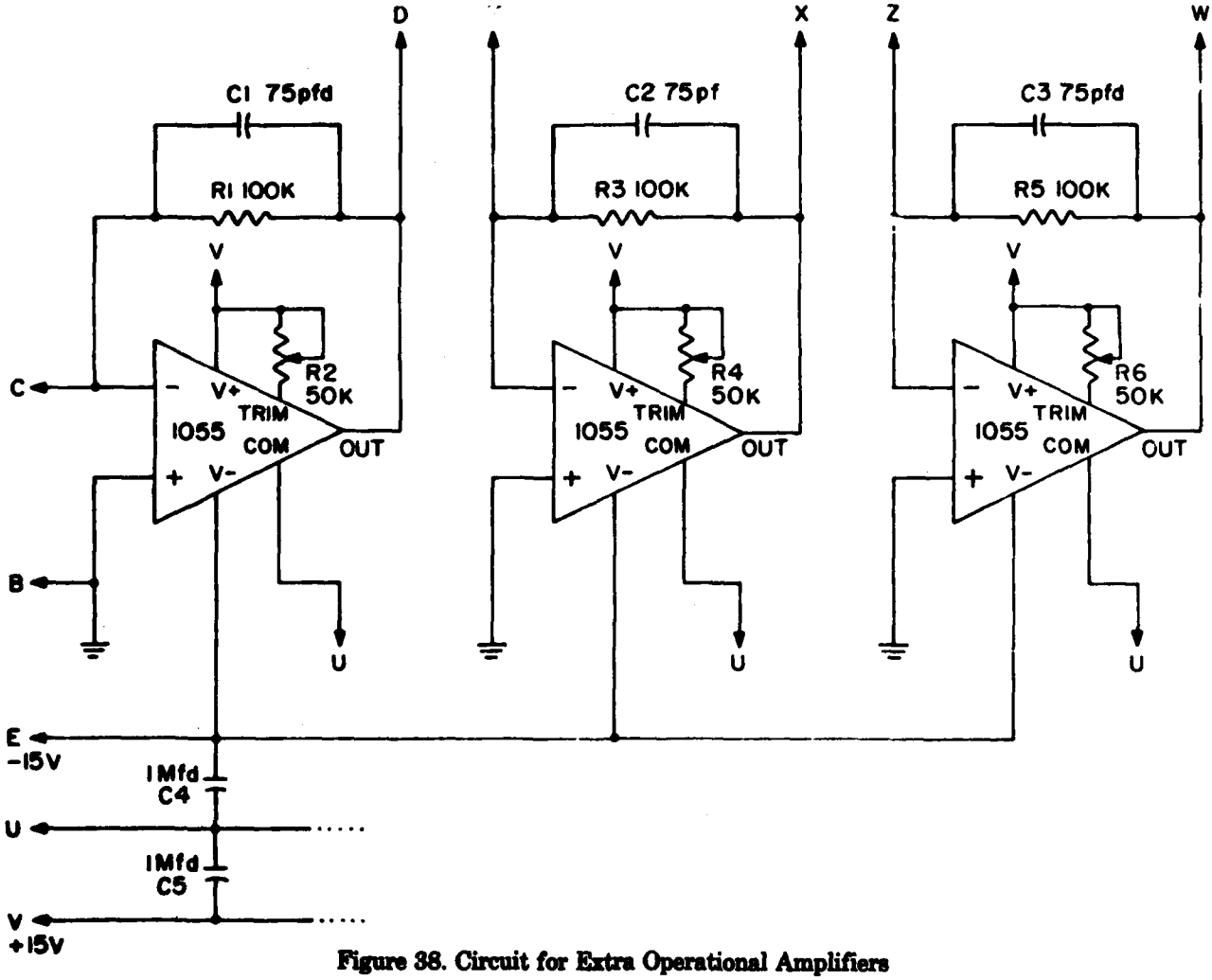


Figure 38. Circuit for Extra Operational Amplifiers

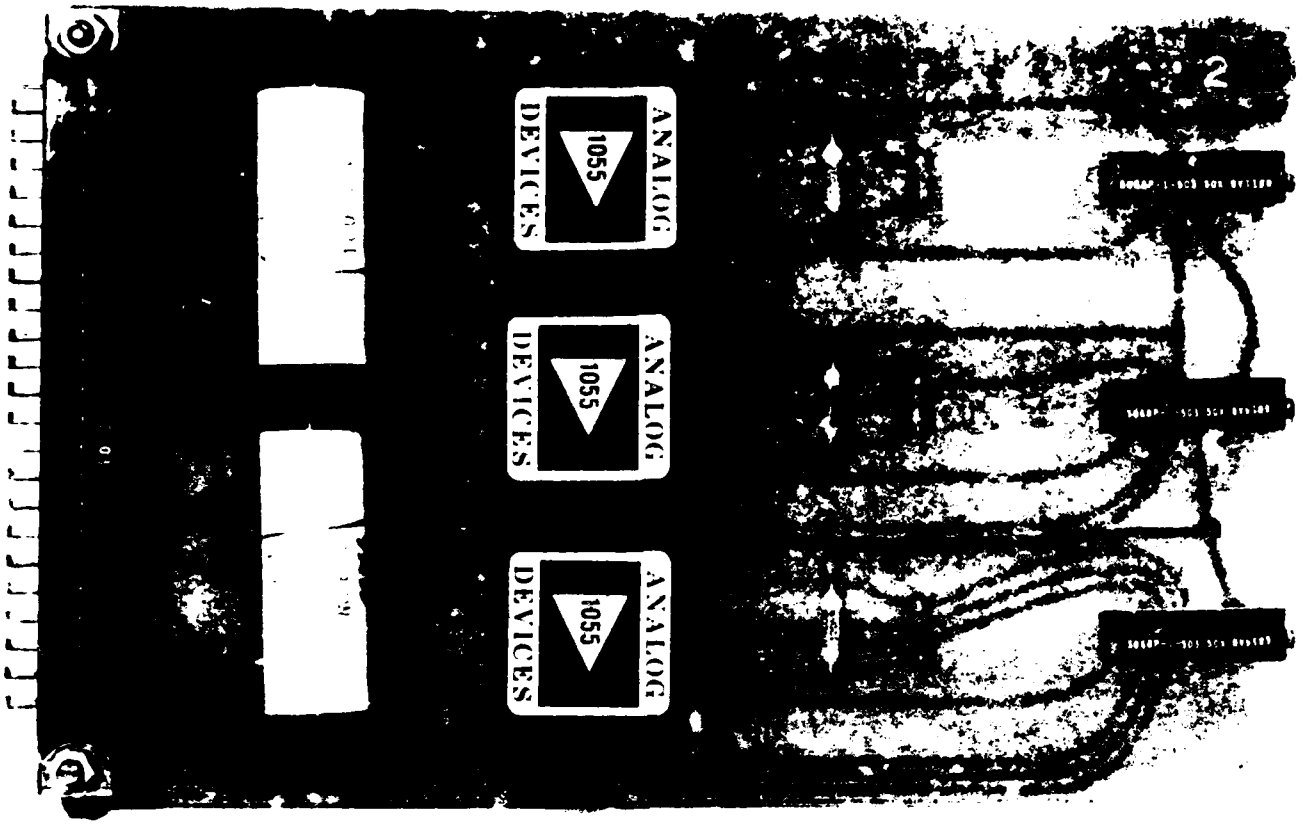


Figure 39. Board for Extra Operational Amlifiers (component side)

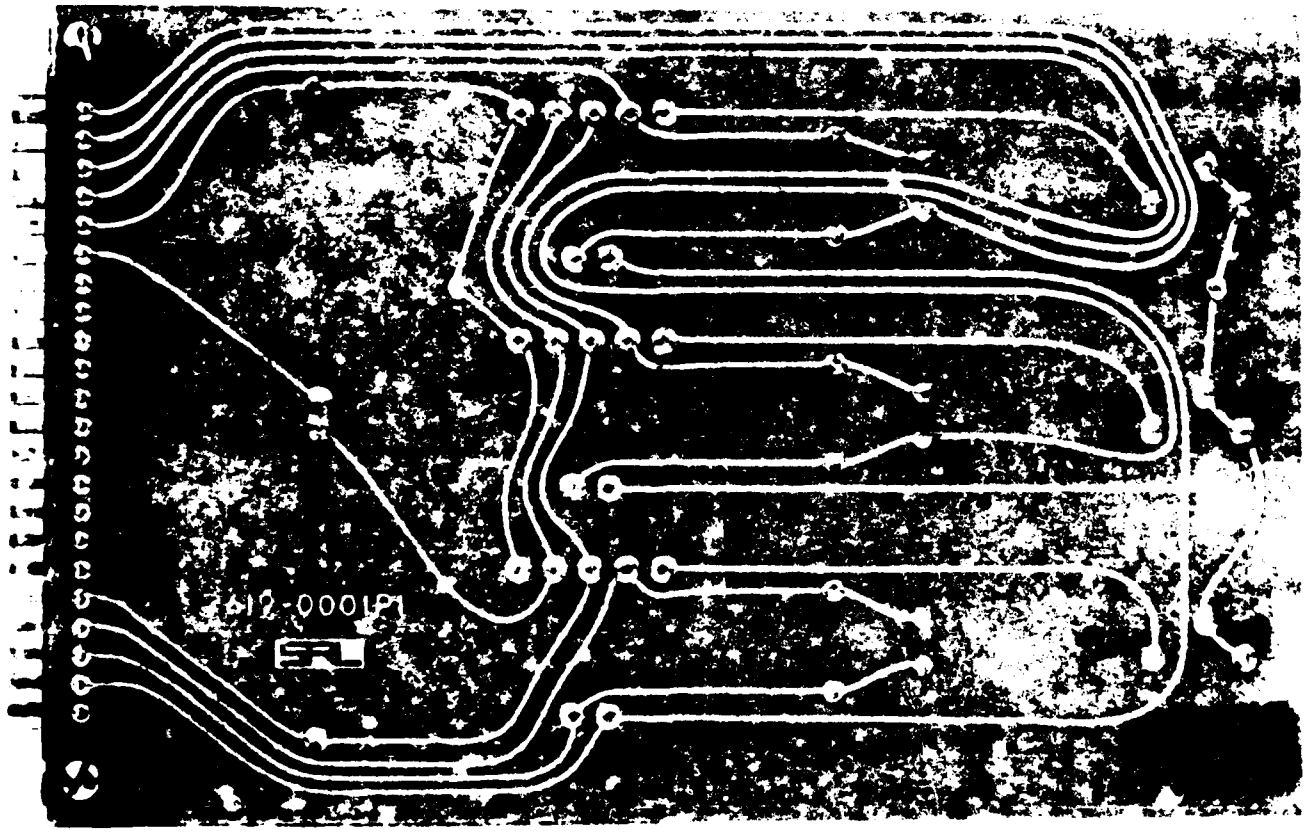


Figure 40. Board for Extra Operational Amplifiers (foil side)

Table 15. Components for the Extra Operational Amplifier Circuits

Designation	Description
C1,2,3,	75 pF ceramic capacitor
C4,5	1 μF mylar capacitor
OA1,2,3	Analog Devices 1055 operational amplifier
R1,3,5	100 kΩ , 1/8 W, 1% film resistor
R2,4,6	50 kΩ Bourns 3068P-1-503 potentiometer

NEON LAMP DRIVERS

Each neon lamp is controlled by a portion of a neon lamp driver board. There are ten circuits, as shown in Figure 41, on each board. Pictures of the circuit boards are shown in Figures 42 and 43, and the components for a single circuit are listed in Table 16. The boards are located underneath each bay and are visible with the drawer pulled out. There are 17 boards (designated W1 through W17) to control the lamps in each bay. Figure 44 shows the lamp driver board locations. Table 17 gives the card location and pin number for each neon lamp driver. The connection between jacks 31 through 36 and the neon lamp driver boards (W1 through W17) can be found in the C³ Wiring Manual.

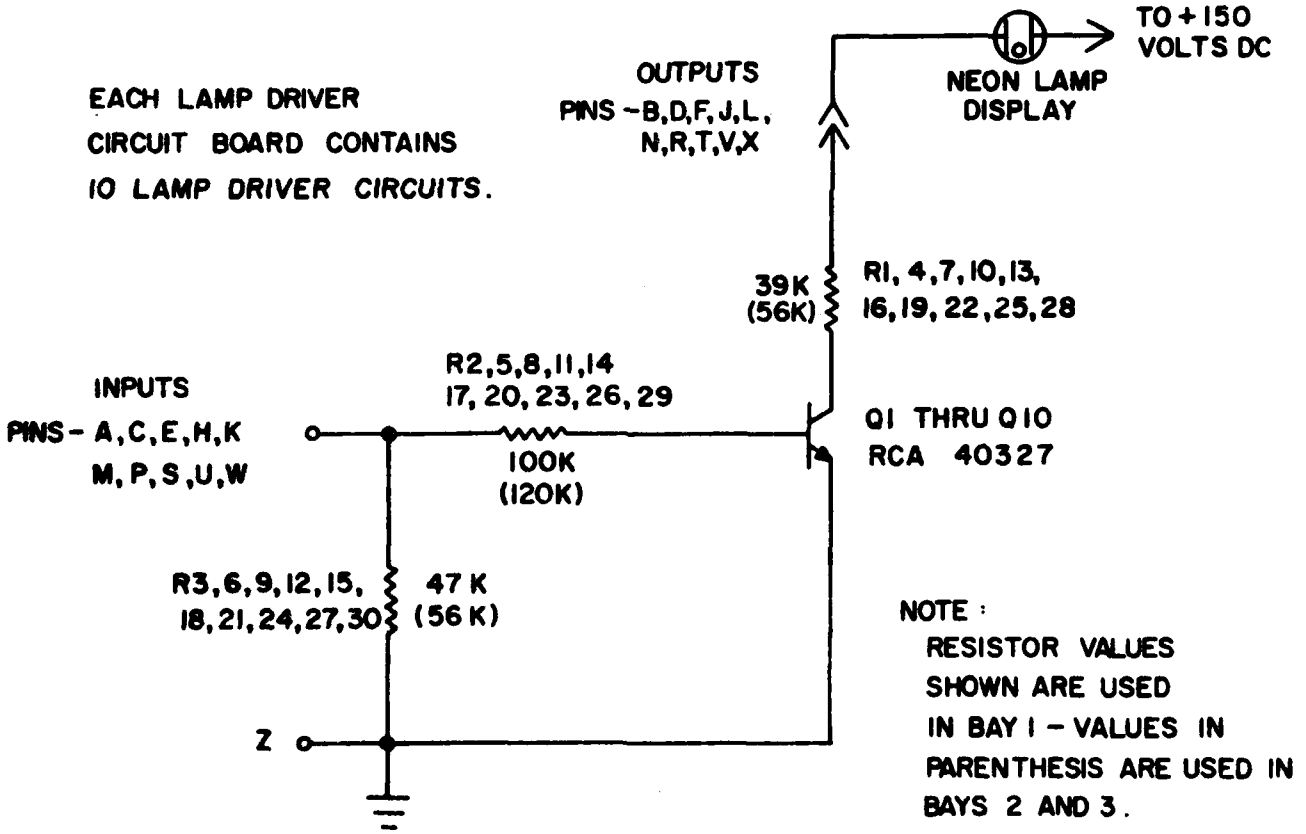


Figure 41. Neon Lamp Driver Circuit

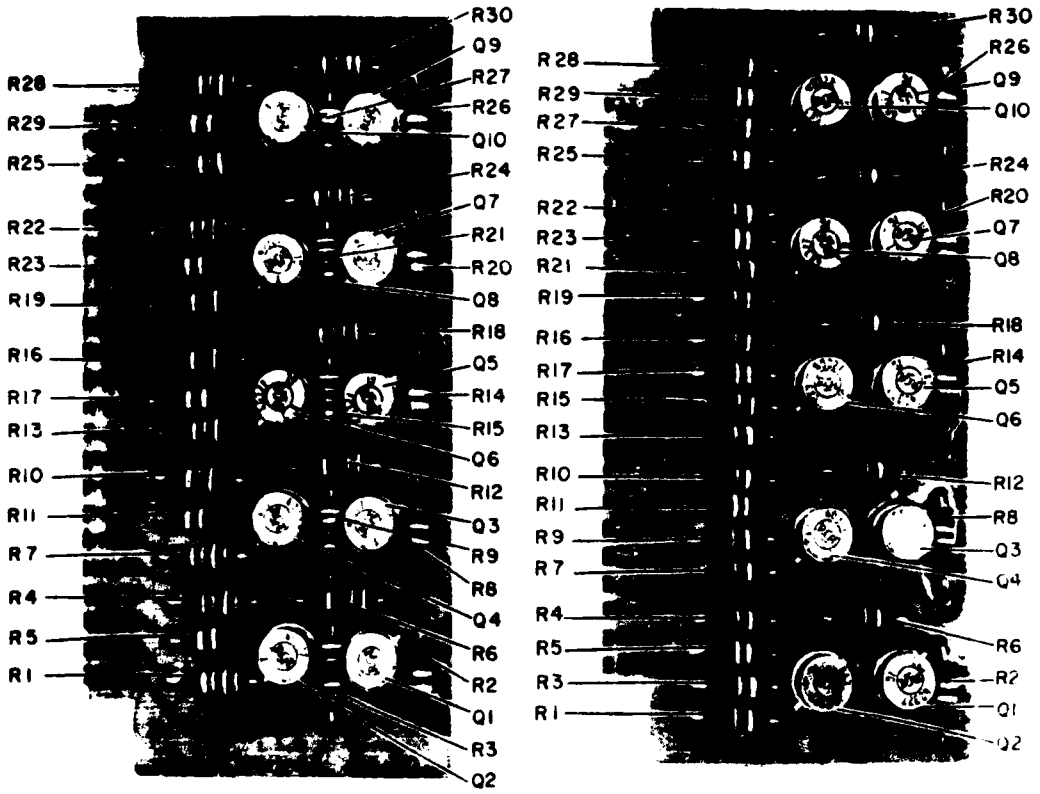


Figure 42. Neon Lamp Driver Boards (component sides)

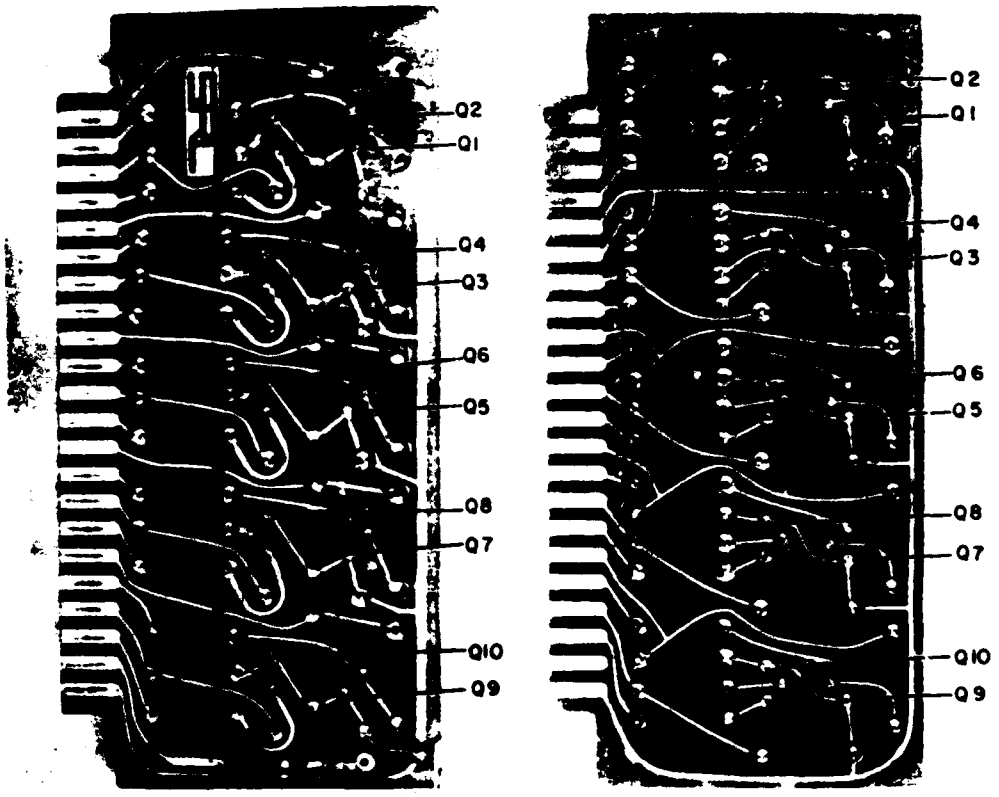


Figure 43. Neon Lamp Driver Boards (foil sides)

Table 16. Components for a Neon Lamp Driver Circuit

Designation	Description
Q1	RCA 40327 NPN transistor
R1	39 kΩ (56kΩ) resistor
R2	100 kΩ (120 kΩ) resistor
R3	47 k Ω (56 k Ω) resistor

NOTE: All resistors are 1/2 watt, 10% tolerance. (Values shown in parentheses are those for bays 2 and 3 which differ somewhat from those of bay 1).

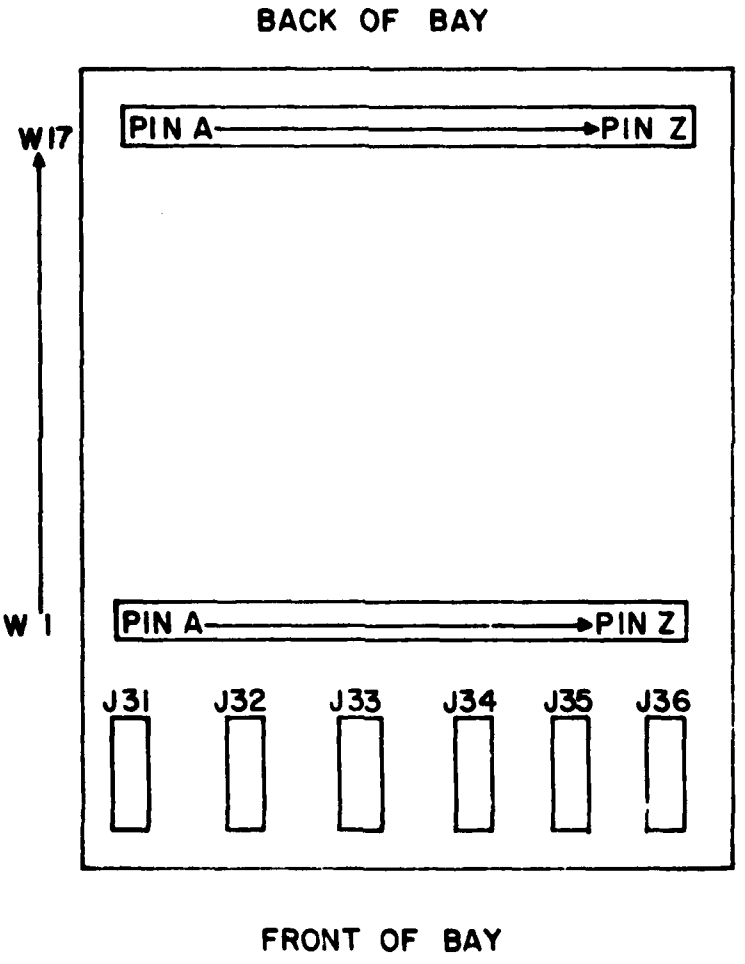


Figure 44. Neon Lamp Driver Board Locations

POWER SUPPLY ISOLATION

Capacitance isolation is employed for each of the + 12, − 12, + 15, and − 15 volt power supplies to the syncoder circuit boards. In bay 1 this is accomplished by soldering the capacitors directly to the connector pins. In bays 2 and 3, the 17th slot of rows A, B, C, D, E, and F each contains a circuit board with the capacitors isolating each of the four power supply lines for that row of syncoder boards. These circuits are not described in any further detail in this report.

Table 17. Neon Lamp Driver Locations

Card	Pin									
	B	D	F	J	L	N	R	T	V	X
W1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
W2	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
W3	A21	A22	A23	A24	A25	A26	A27	A28	B1	B2
W4	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
W5	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22
W6	B23	B24	B25	B26	B27	B28	C1	C2	C3	C4
W7	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
W8	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24
W9	C25	C26	C27	C28	D1	D2	D3	D4	D5	D6
W10	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
W11	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26
W12	D27	D28	E1	E2	E3	E4	E5	E6	E7	E8
W13	E9	E10	E11	E12	E13	E14	E15	E16	E17	E18
W14	E19	E20	E21	E22	E23	E24	E25	E26	E27	E28
W15	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
W16	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20
W17	F21	F22	F23	F24	F25	F26	F27	F28		

SYNAPSE BUTTONS

A synapse button is used to connect selected syncoder analog output signals and sample-and-hold voltages to syncoder summing junctions. (Not all such connections must be made through synapse buttons, only those which are to be "gated", i.e. controlled, by syncoder pulse outputs.) The synapse button circuit board, which contains four separate circuits, is mounted in clear plastic with its connector (wires terminated with patch panel plugs) extending from the body. When inserted in a network, the synapse buttons hang on the front of the large patch panel with the other connectors. A single pulse input lead simultaneously controls all four circuits. The four switches may be plugged into four different voltage sources and may be used as inputs to four different synapse integrators. That is, the synapse button functionally resembles a four-pole, single-throw relay.

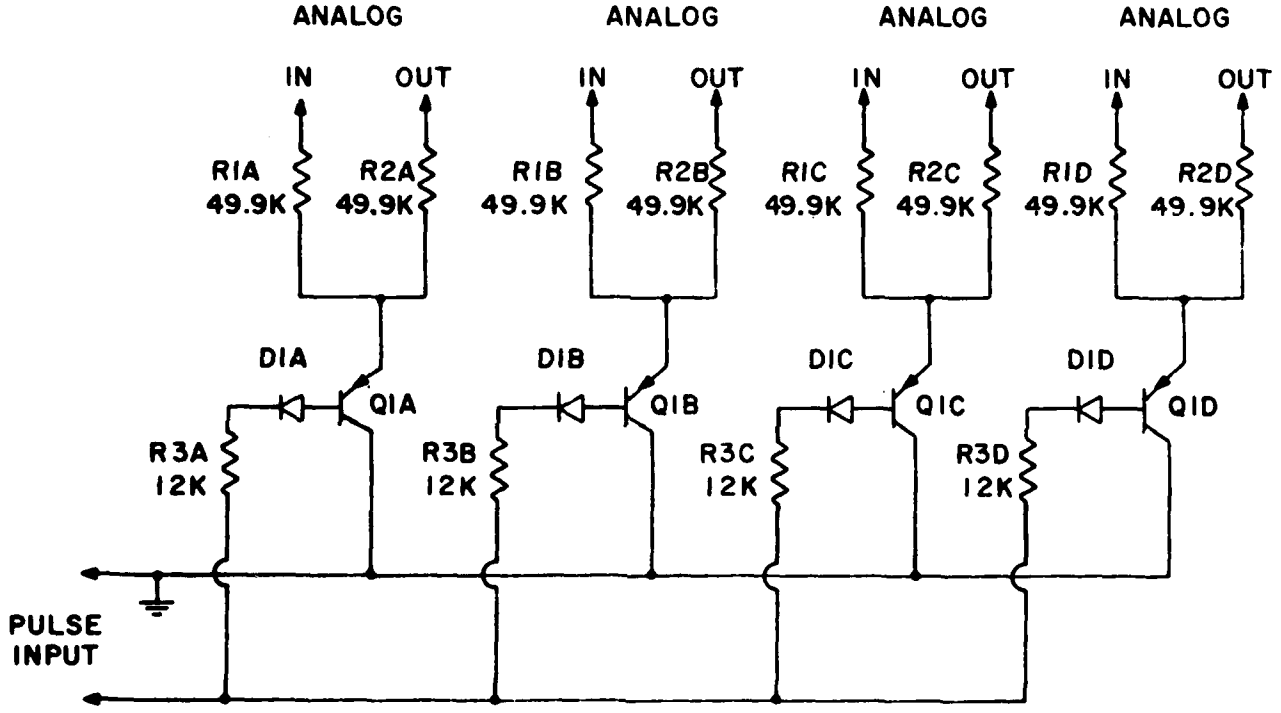
Each circuit is a symetrical shunt type switch whose output must be connected to the summing junction of an inverting operational amplifier for proper operation. The circuit schematic is shown in Figure 45; the circuit board, prior to being encapsulated in clear plastic, is pictured in Figure 46; and the components are listed in Table 18. Resistor R2 is connected to the virtual ground summing junction of a synaptic integrator, and R1 is connected to an analog voltage source called the weighting voltage. When the pulse input is low (– 12 volts), D1 is forward biased and transistor A1, operating in an inverted mode (using its collector as its emmitter), is saturated. The 2N4058 transistor has a current gain of three in the inverted mode, but an extremely low saturation voltage of less than three millivolts. Thus, when Q1 is saturated, any current through R1 resulting from the weighting voltage is shunted to ground through Q1A and has no effect on the op amp.

When the pulse input goes high (+ 12 volts), diode D1 is reverse biased and transistor Q1 turns off. Because Q1 is operated with an open base during its off state, the turn-off time constant is approximately 30 microseconds. That is the time it takes the collector current to discharge the stored charge in the base region so that the transistor can reach cut-off. Once Q1 is cut off, then the weighting voltage is connected to the summing junction through R1 and R2, and a current proportional to the weighting voltage is injected into the summing junction. Thus during a pulse, current resulting from the weighting voltage is injected into the summing junction, and between pulses, that current is shunted to ground through Q1.

The synapse button is not an ideal switch. In the off state the signal is attenuated 54 dB relative to the on state when a negative weighting voltage is applied. When a positive weighting voltage is applied, the off state provides greater attenuation. An additional departure from ideality exists in the transition from the off state to the on state and back to the off state. Voltage spikes are produced on the leading and trailing edges of the switching pulses; however, the feedback capacitors which make the syncoder input operational amplifiers "leaky integrators" diminish the voltage spikes significantly. Measurements made on the Mode 5 Syncoder Board with a 75-picofarad feedback capacitor showed that the worst case occurs when the weighting voltage is zero. In this case a – .5 volt

spike on the leading edge of the switching pulse followed by a + .5 volt spike on the trailing edge is added to the S(t) voltage value. Measurements were made at the output of the first operational amplifier. A weighting voltage of − 10 volts produces a trailing edge spike of 0.3 volts while a + 10 volts weighting voltage produces no spike whatsoever. These measurements were all made using the typical 75 picofarad feedback capacitor. A larger capacitance will reduce the voltage spike even further.

Voltage spikes would be a problem only if several synapse buttons were summed together at one syncoder and gated simultaneously. While it is common for the on states of two or more syncoders to overlap, it is highly unlikely that the leading and/or trailing edges to exactly coincide. It is necessary for the operator to recognize that the on states of two or more synapse buttons may overlap. Weighting voltages may take on values between + 10 volts and − 10 volts. If the instantaneous summation of weighting voltages seen by a given syncoder exceeds ± 12 volts, the output comparator (Mod 5) will saturate and erroneous results occur. The same caution applies to all syncoder boards.



ALL TRANSISTORS - 2N4058 T. I.
ALL DIODES - IN4154

Figure 45. Synapse Button Circuit

Table 18. Components for the Synapse Button Circuit

Designation	Description
D1	1N4154 diode
Q1	2N4058 T.I. PNP transistor
R1,2	49.9 kΩ , 1/8 W, 1% film resistor
R3	12 kΩ , 1/8 W, 5% resistor

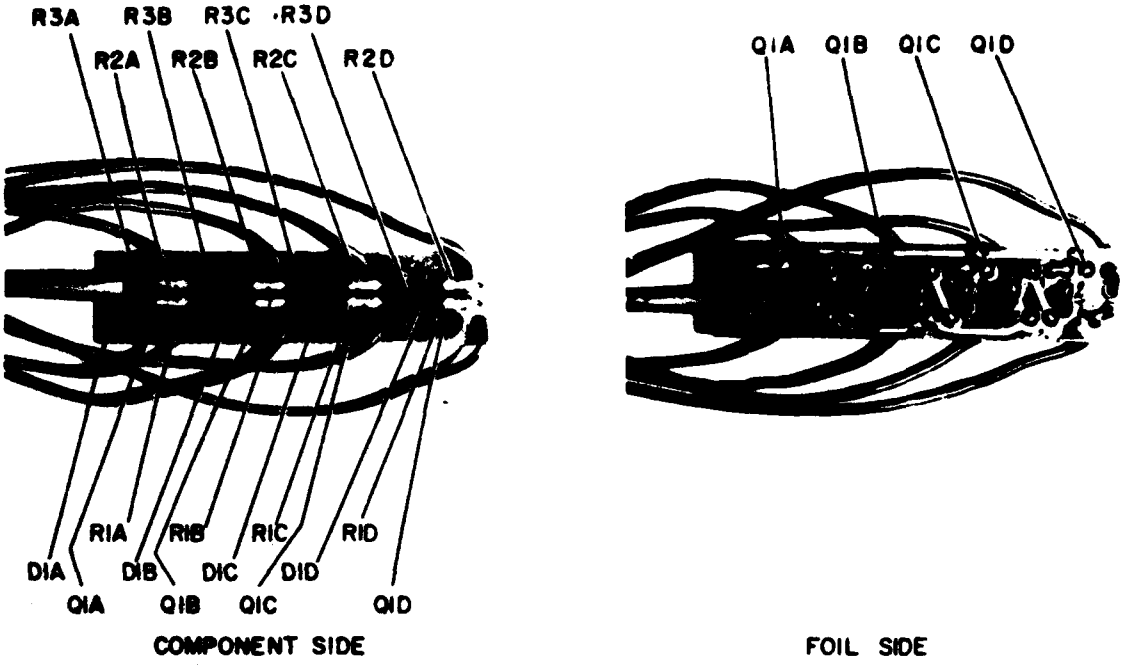


Figure 46. Synapse Button Circuit Board

POTENTIAL APPLICATIONS

The C^3 System is a unique general purpose signal processing device; however, its special attributes are best applied to multicomponent time-varying signals. C^3 can process many signals simultaneously - performing a simulated neural tranformation, differentiating, integrating, summing and/or comparing selected combinations of signals. The use of plug-in circuit boards with tunable parameters and patch panels with patch cords incorporating electronic components such as resistors or capacitors makes C^3 a very flexible system. Not only can C^3 be programmed to perform a variety of functions, but preprocessing of its input and postprocessing of its output can further increase its capabilities.

C^3 can accept a large number of inputs. The actual number would depend on the processing desired, ultimately being limited by the syncoders available. Our research has concentrated on acoustic signals, and the electrical signal from a microphone is fed through a special preprocessor called an analog cochlea. Although many versions of analog cochleas exist, each is basically a tapped delay line (cascaded, low-pass) filter set. (Glaesser et al, 1963; Steer et al, 1976) Our current version sends 48 time-varying signals to C^3; however, only 24 are being processed at the present time.

Although C^3 can be programmed to detect certain combinations of coincidence, this is also limited by the number of syncoders available. But it can supply a large number of outputs (both analog and pulse) to other devices such as a digital computer or a special hardware device. With some special processing of pulse outputs, 32 channels are fed to a PDP-11/20 digital computer for data reduction. Recently, the primary data reduction technique, reference pattern correlation, has been realized in a real-time hardware device.

This potential on-line pattern recognition system could fit many applications. In the acoustics area, we have used it for speech recognition (Warmuth, 1978) and target identification using sonar or doppler radar returns. As a further example, with the appropriate tranducers and preproccesors, such as a spectral colorimeter or a photo matrix assembly, classifying the color or the shape of subjects could be investigated.

RECOMMENDATIONS

The C^3 System was developed as a tool for the study of large neuron networks which would require prohibitively large amounts of computer time to simulate in software. The need for a large number of individual neuron model units, coupled with the ability to readily interconnect and control them has been met with the C^3 System. However, several recommendations can be made for future consideration concerning the general system.

First, the ability of the C^3 System to accurately model a neuron network is dependent on the ability of the syncoder to model an individual neuron. Therefore, a continued effort should be made to improve the syncoder as a neuron model. The incorporation of stochastic principles, which would make the simulation more realistic, should be included in the next modification.

Second, the existing system is physically very large. A potential solution to this problem would be to develop an intergrated circuit (IC) containing one or more syncoders in a single IC package. This would reduce the size of the system as well as its power requirements.

Finally, the real value of the C^3 System is in its flexibility and the ease of changing networks. Thus, it is important to maintain a reasonable number of available syncoders for additions and changes. As a given network grows, large numbers of syncoders may become tied up in subnetworks which will never be changed. As these static subnetworks are identified, an analysis should be made of their functioning as a whole; and a separate special purpose hardware circuit built to perform that function. Such a circuit might not utilize syncoders at all, but would produce the same outputs as the original syncoder subnetwork. This would free many syncoders and help maintain the capacity and the flexibility of the C^3 System in its use as a tool for neuron network experiments.

BIBLIOGRAPHY

Gruenke, Roger A., *Information Processing in Small Syncoder Networks,* March 1967, AMRL-TR-67-104, Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Hartrum, Thomas C. and Robert Burckle, "The Stochastic syncoder as a Neuron Model" *Proc. of IEEE 1977 National Aerospace & Electronics Conf.,* Dayton, OH, May, 1977.

Leet, Duane G., *A Primary Auditory Nerve Model,* October 1976, AMRL-TR-76-84, Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Martin, William K., *Investigation of the Characteristics of Syncoder Networks,* September 1967, Masters Thesis GE/EE/67S-3, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio.

Miller, John H., *Investigation of the Effects of Noise on the Encoding Function of Syncoders,* June 1974, Masters Thesis GE/EE/74-13, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio.

Mundie, J. Ryland, "Neural Calculus, "*Biocybernetics of the Central Nervous System,* Lorne D. Proctor, Ed., Little; Brown, and Co., Boston, 1969.

Mundie, J. R., J. C. Rock, A. J. Goldstein, "Signal Processing Principles Revealed by an auditory System Model, "*Kybernetic and Bionics (Cybernetics and Bionics) - Proceedings of the 5th Congress of the Duetsche fur Kybernetik* held at Nuremberg, March 28-30 1973, R. Oldenbourg, Munich, Germany, 1974.

Zellmer, Richard B., *An Investigation of the Syncoder as a Pulse-Interval Processing Device,* June 1972, Masters Thesis GGC/EE/72-19, Air Force Institute of Technology, Wright-Patterson Air Force Base, OH.

REFERENCES

Glaesser, E., Caldwell, W.F., and Stewart, J.L., June 1963, *An Electronic Analog of the Ear,* AMRL-TDR-63-60, AD411320 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Gruenke, Roger A. and Mundie, J. R., May 1968, *Design and Operation of Root C, A Small Syncoder Network Simulator,* AMRL-TR-67-236, AD672976 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Mathur, Dilip K. and Henrichon, E. G., Jr., March 1971, *Mathematics of Syncoders,* AMRL-TR-70-35, AD721225 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Rock, James C., January 1973, *Recursive Plane Analysis: Its Application to the Study of Phase-Locking in Non-Uniform Signal-Dependent Sampling Techniques,* AMRL-TR-72-34, AD756918 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Steer, Robert W., Rock J.C., Mundie, J.R., and Osborne, D., January 1976, *Design of an Active COC Filter for Audio Frequency Signal Processing* AMRL-TR-75-78, ADA022903 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.

Warmuth, Donald B., June 1978, *Automatic Recognition of Synthetic Speech using an Electronic Model of the Middle and Inner Ear,* Doctoral Dissertation AFIT/DS/EE/78-3, Air Force Institute of Technology, Wright-Patterson Air Force Base, Ohio.

Zielkin, Marvin C. and Mundie, J. R., March 1971, *Encoding Function of Syncoders, AMRL-TR-70-119, AD724072 Aerospace Medical Research Laboratory, Wright-Patterson Air Force Base, Ohio.*

☆ U.S. GOVERNMENT PRINTING OFFICE: 759-108/1307

END

FILMED

1-84

DTIC